JSS MAHAVIDYAPEETHA

JSS SCIENCE AND TECHNOLOGY UNIVERSITY

SRI JAYACHAMARAJENDRA COLLEGE OF ENGINEERING

- Constituent College of JSS Science and Technology University
- Approved by A.I.C.T.E
- Governed by the Grant-in-Aid Rules of Government of Karnataka
- Identified as lead institution for World Bank Assistance under TEQIP Scheme

JSS MAHAVIDYAPEETHA

JSS SCIENCE & TECHNOLOGY UNIVERSITY, MYSURU

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

COMMUNICATION LAB –II
(20EC58L)

Prepared by
Dr. Gayitri H M

Vision statement of the department of E&CE

Be a leader in providing globally acceptable education in electronics and communication engineering with emphasis on fundamentals-to-applications, creative-thinking, research and career building.

Mission statement of the department of E&CE

1. To provide best infrastructure and up-to-date curriculum with a conducive learning environment.

2. To enable students to keep pace with emerging trends in Electronics and Communication Engineering.

3. To establish strong industry participation and encourage student entrepreneurship.

4. To promote socially relevant eco-friendly technologies and inculcate inclusive innovation activities.

Objectives

1. Familiarize the students with basics of digital communication systems.

2. Integrate theory with experiments so that the students appreciate the knowledge gained from the theory course.

3. Students should able to design and develop various waveform coding circuits.

Course Outcomes

After studying this course the students shall be able to:

1. Analyze various digital modulation and demodulation circuits and analog to digital and DAC circuits

2. Design various digital modulation circuits and simulate different waveform coding techniques using software simulation tools.

3. Demonstrate the working of wireless communication system and microwave experiments by using microwave bench setup

LIST OF EXPERIMENTS

1. Analog to digital converter using Flash type ADC
2. Digital to analog converter using binary weighted resistors
3. Transistor Mixer
4. ASK modulator and Demodulator using discrete components and Kit
5. FSK modulator and Demodulator using discrete components and Kit
6. PSK modulator and demodulator using discrete components and Kit
7. Time division multiplexing and de-multiplexing
8. Pulse code modulation using Matlab simulator
9. Delta modulation and demodulation using Matlab simulator
10. Adaptive delta modulation and demodulation using Matlab simulator
11. OFC Kit experiments
12. Wireless communication and antenna experiments using microwave bench setup.

NOTE: A minimum of 10(Ten) experiments have to be performed and recorded by the candidate to attain eligibility for University Practical Examination

Course articulation matrix

	PO1	PO2	PO3	PO4	PO5	PO6	PO9	PO10	PS11	PSO2	PSO3	PSO3
CO1		3										
CO2			3									
CO3		3	3		3	3	2		3		3	2
EC46L(Avg)		3	3	**3**	3	3	2		3		3	2

Experiment No.1

A/D Converter

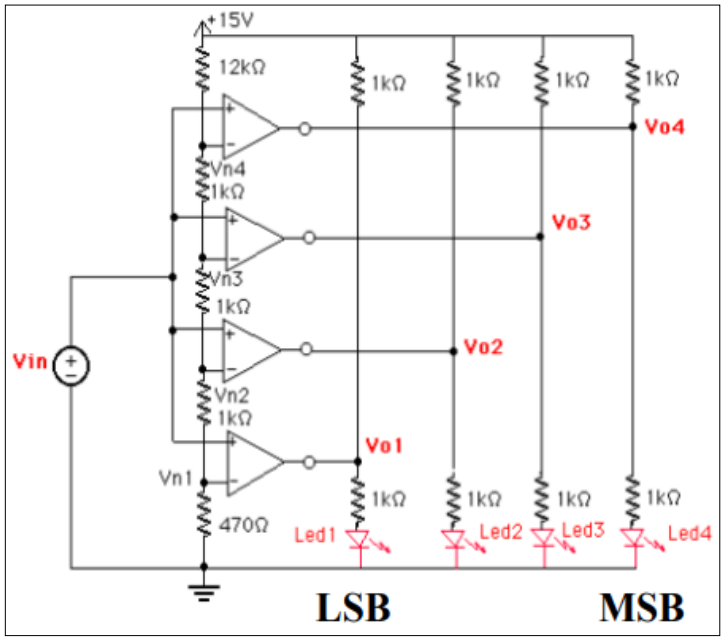
AIM: Design the A/D converter circuit and describe their operation.

Components required : Resistors, Op-amp, Power supply.

THEORY:

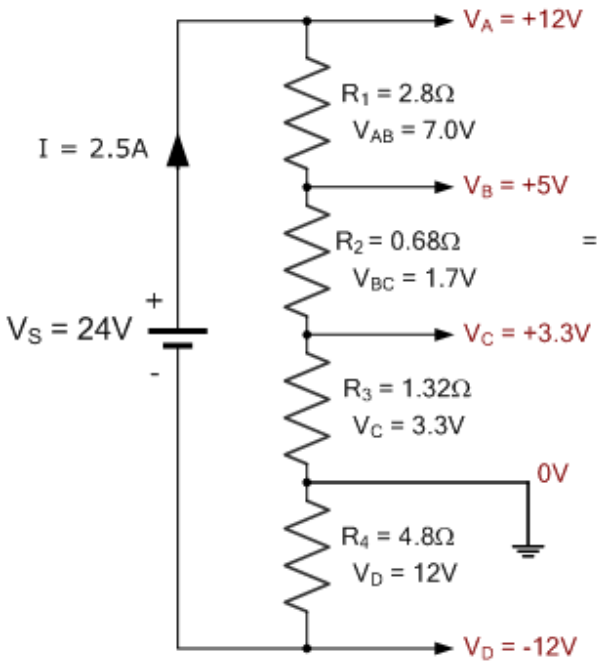
Flash Type ADC is based on the principle of comparing analog input voltage with a set of reference voltages. To convert the analog input voltage into a digital signal of n-bit output, $(2^n - 1)$ comparators are required. Flash Converter the circuit consists of 4 comparators whose inverting inputs are connected to a voltage divider. A comparator is basically an operational amplifier used without feedback. The outputs of the comparators correspond to a digital word. When the input rises above Vn1, the first comparator will switch to a high output voltage causing the LED to light up, indicating a (0001). For larger input voltages the output of other comparators will switch high as well. For large input voltages (above Vn3) all comparators will be high corresponding to (1111) digital output.

CIRCUIT DIAGRAM:



Vn1=Vs(R5)/(R1+R2+R3+R4+R5)=15*470/(12+1+1+1+470)=0.455v
Vn2=Vs(R4)/(R1+R2+R3+R4)=15*1/(12+1+1+1)= 1V
Vn3=Vs*R3/(R1+R2+R3)=15*1/(12+1+1)=15/14=1.07V
Vn4=Vs*R2/(R1+R2)=15*1/(12+1)=15/13=1.15V

voltage levels of -12V, +3.3V, +5V and +12V if the total power supplied to the unloaded voltage divider circuit is 24 volts DC, 60 watts.



$$P = V^*I$$

$$\text{Therefore: } I = \frac{P}{V} = \frac{60}{24} = 2.5A$$

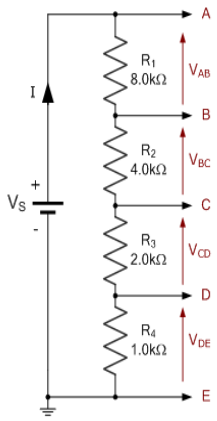
$$R_1 = \frac{V_A - V_B}{I} = \frac{12 - 5}{2.5} = 2.8\Omega$$

$$R_2 = \frac{V_B - V_C}{I} = \frac{5 - 3.3}{2.5} = 0.68\Omega$$

$$R_3 = \frac{V_C - 0}{I} = \frac{3.3}{2.5} = 1.32\Omega$$

$$R_4 = \frac{V_D - 0}{I} = \frac{12}{2.5} = 4.8\Omega$$

Voltage Tapping Points in a Divider Network



Consider a long series of resistors connected to a voltage source, V_S. Along the series network there are different voltage tapping points, A, B, C, D, and E.

The total series resistance can be found by simply adding together the individual series resistance values giving a tot resistance, R_T value of 15kΩ. This resistive value will limit the flow of current through the circuit produced by the supply voltage, V_S.

The individual voltage drops across the resistors are found using the equations above, so $V_{R1} = V_{AB}$, $V_{R2} = V_{BC}$, $V_{R3} = V_{CD}$, and $V_{R4} = V_{DE}$.

The voltage levels at each tapping point is measured with

$$R_T = R_1 + R_2 + R_3 + R_4 = 8k\Omega + 4k\Omega + 2k\Omega + 1k\Omega = 15k\Omega$$

$$V_{R1} = V_{AB} = V_S\left(\frac{R_1}{R_T}\right) = 15\left(\frac{8000}{15000}\right) = 8\text{volts}$$

$$V_{R2} = V_{BC} = V_S\left(\frac{R_2}{R_T}\right) = 15\left(\frac{4000}{15000}\right) = 4\text{volts}$$

$$V_{R3} = V_{CD} = V_S\left(\frac{R_3}{R_T}\right) = 15\left(\frac{2000}{15000}\right) = 2\text{volts}$$

$$V_{R4} = V_{DE} = V_S\left(\frac{R_4}{R_T}\right) = 15\left(\frac{1000}{15000}\right) = 1\text{volts}$$

PROCEDURE:

1. Connect the opamp in comparator configuration and provide the reference input of +15V DC supply.
2. By varying the input voltage observe the output voltage of the comparator versus LED output and tabulate 4bit digital output.

RESULT: ADC circuit is designed and verified

Experiment No.2

D/A Converter

AIM: Design the D/A converter circuit and describe their operation.

THEORY: The purpose of a digital-to-analog converter is to convert a binary word to a proportional current or voltage. The binary weighted resistors produce binary-weighted current which are summed up by the op-amp to produce proportional output voltage. The binary word applied to the switches produces a proportional output voltage. Several different binary codes such as straight binary, BCD and offset binary are commonly used as inputs to D/A converters. The operational amplifier is employed as a summing amplifier, which produces the weighted sum of these input voltages. the summing amplifier multiplies each input voltage by the ratio of the feedback resistor R_F to the corresponding input resistor R_{IN}. In this circuit R_F R_{IN} 1kΩ and the input resistors range from 1 to 8 kΩ . The D input has R_{IN} = 1KΩ, so the summing amplifier passes the voltage at D with no attenuation. The C input has R_{IN} =2 kΩ, so that it will be attenuated by. Similarly, the B input will be attenuated by ¼ and the A input by 1 /8. The amplifier output can thus be expressed as

$$V_{OUT} = - (V_D + 1/2\ V_C + 1/4 V_B + 1/8\ V_A)$$ [1]

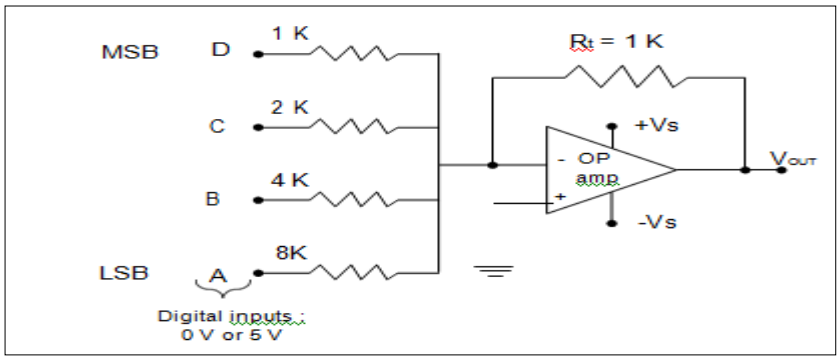
The negative sign is present because the summing amplifier is a polarity- inverting amplifier,

Clearly, the summing amplifier output is an analog voltage which represents a weighted sum of the digital inputs. The output is evaluated for any input condition by setting the appropriate inputs to either 0 V or 5 V. For example, if the digital input is 1010, then $V_D = V_B = 5V$ and $V_C = V_A = 0V$. Thus, using equation

$$V_{OUT} = - (5V + OV + ¼ \times 5V + OV)$$
$$= - 6.25V$$

The resolution of this D/A converter is equal to the weighting of the lSB,which is 1/8 × 5V = 0.625 V. The analog output increases by 0.625 V as the binary input number advances one step.

CIRCUIT DIAGRAM:



DAC circuitry using op-amp with binary weighted resistors.

PROCEDURE:

1. Connect the inputs A,B,C, and D have values of either 0 V or 5 V.
2. Connect the opamp as summing amplifier and tabulate the result and find the resolution.

RESULT: DAC circuit is designed and verified.

Experiment No.3

TRANSISTOR MIXER

AIM: To set up a transistor mixer circuit to produce IF from RF and oscillator frequency inputs and to measure the conversion transconductance.

OBJECTIVES:

After completing this experiment, the students will be able to a) set up a transistor mixer circuit and to b) study the relation between the RF, oscillator frequency and IF and to c) measure the conversion transconductance.

COMPONENTS AND EQUIPMENTS REQUIRED:

Sl. No.	Item & Specification	Quantity
1	Resistor- 22K, 33K, 3.3K	1No. each
2	Transistor BF194	1No.
3	Capacitor- 0.1μF	1No.
4	IFT	1No.
5	Signal Generator	2Nos.
6	CRO	1No.
7	Power Supply- =12V	1No.
8	Multimeter	1No.
9	Bread Board	1No.
10	Wires and probes	

THEORY:

Mixer or frequency convertor is actually a non linear resistor having two sets of input terminals and one set of output terminal. The two inputs to the mixer are the input signal and the local oscillator signal. The output of the mixer contains many frequencies including the sum and difference frequencies between the two input signals. The mixer output is commonly tuned to the difference frequency. This frequency is called the intermediate frequency (IF).

The input to the mixer is the input signal voltage with magnitude V_S and frequency f_S. The output is usually a current component at IF frequency having a magnitude I_{IF} proportional to V_S. The proportionality constant is called transconductance and is given by

$$g_C = I_{IF} / V_S$$

The conversion transconductance of a transistor mixer is of the order of 6ms. Mixing takes place when the transconductance of the mixer is caused to vary with the local oscillator voltage.

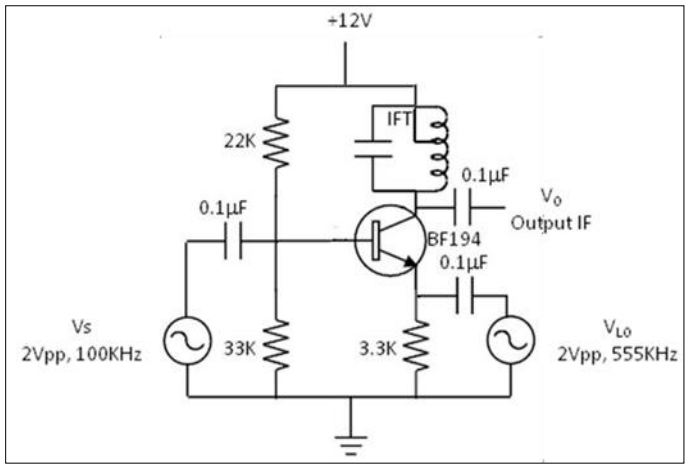
PROCEDURE:

1. Test all the components and probes.
2. Set up the circuit as shown in figure on a breadboard.

3. Switch on the power supply.
4. Check the dc conditions of the transistor and make sure that it is working in the active region.
5. Feed a 2Vpp, 100KHz sine wave signal at the base of the transistor as shown in figure.
6. Feed a 2Vpp, 555KHz sine wave signal at the emitter of the transistor as shown in figure.
7. Observe the output waveform on a CRO and measure the frequency. Adjust the IFT to obtain 455KHz as the peak output frequency.
8. Plot the input/output waveforms.
9. Measure the output ac current (I_{IF}) and the input ac voltage (V_S) using a multimeter. Calculate the transconductance using the equation $g_C = I_{IF}/ V_S$
10. Check the output for 100KHz and 355KHz inputs.

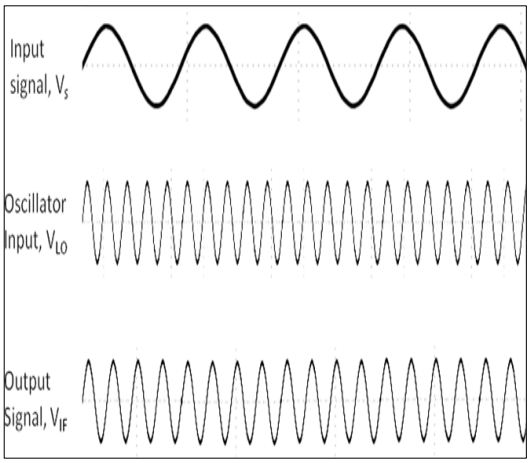
Note: The IFT centre tap point should be connected to Vcc. Connect one of the other two terminals of the IFT primary to the collector of the transistor. Try both terminals and select the one that gives the better output.

Circuit Diagram:



Transistor Mixer

WAVEFORMS:



RESULT:

The Mixer circuit was set up and the waveforms were plotted.

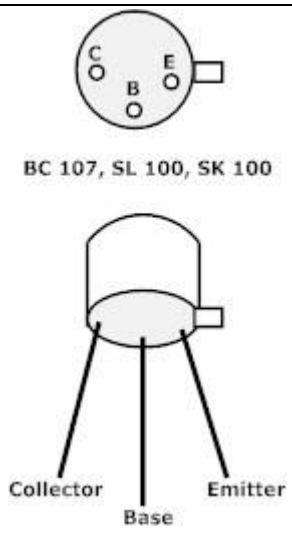
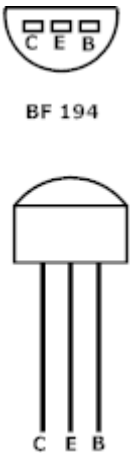
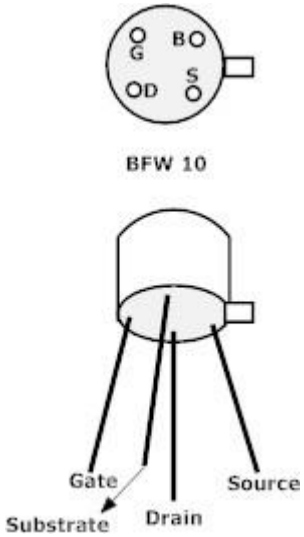
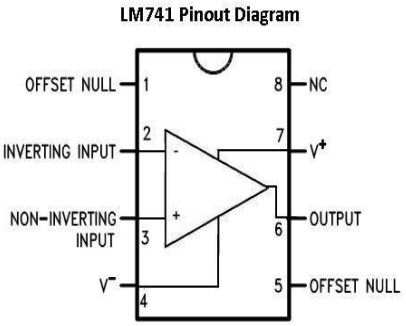
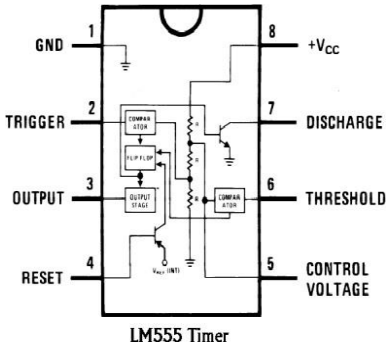
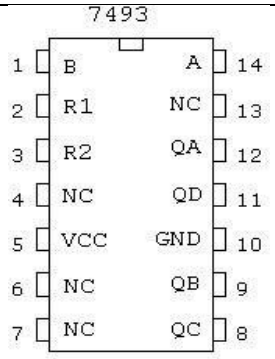
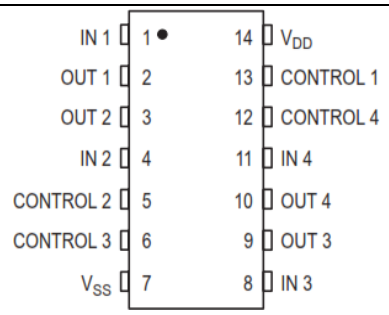
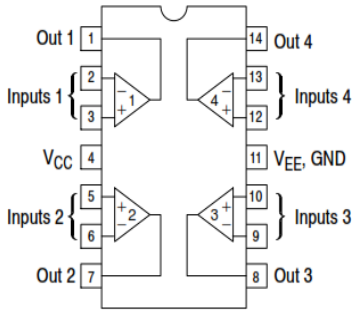
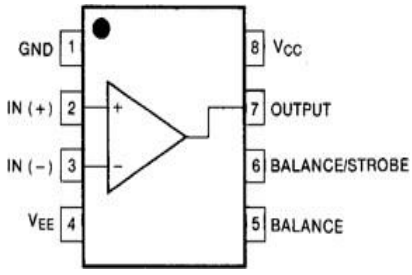
Frequency of the IF signal = ……..

Conversion transconductance, g_C = ……...

INFERENCE:

1) The transistor in a mixer circuit is acting as a non linear resistor.
2) The IF is the frequency difference between the local oscillator frequency f_{LO} and the input signal frequency f_S.

PIN DIAGRAMS

BC 107, SL 100, SK 100	BF 194	BFW 10
		
IC 741	**IC 555**	**IC 7493**
		
CD 4016	**LM 324**	**LM 311**
		

Experiment No.4

ASK MODULATOR AND DEMODULATOR

AIM:

To set up ASK modulator and demodulator circuits and to observe the waveforms.

OBJECTIVES:

After completing this experiment the students will be able to a) Set up ASK modulator and demodulator circuits and b) Identify ASK waveform.

COMPONENTS AND EQUIPMENTS REQUIRED:

Sl. No.	Item & Specification	Quantity
1	Transistor- BC 107	1No.
2	Resistor- 4.7K, 10K, 2.2K, 1K 10K pot	1No. each 1No.
3	Capacitor- 0.01μF	1No.
4	Diode- 1N 4001	1No.
5	Zener Diode- 5Z1	2Nos.
6	IC 741	1No.
7	Signal Generator	2Nos.
8	CRO	1No.
9	Power Supply- +/- 15V, 5V	1No. each
10	Bread Board	1No.
11	Wires and probes	

THEORY:

Amplitude Shift Keying (ASK) is a digital modulation scheme where the binary data is transmitted using a carrier signal with two different amplitude levels. For binary 0 and 1, the carrier switches between these two levels. In its simplest form, a carrier is sent during one input and no carrier is sent during the other. This kind of modulation scheme is called on-off keying.

A simple ASK modulator circuit is shown in figure. Here a sinusoidal high frequency carrier signal is sent for logic ‘0’ (-5V) and no carrier is sent for logic ‘1’ (+5V). The transistor works as a switch closes when the input (base) voltage is +5V (logic ‘1’) and shorts the output. When the input voltage is -5V (logic ‘0’), the switch opens and the carrier signal is directly connected to the output.

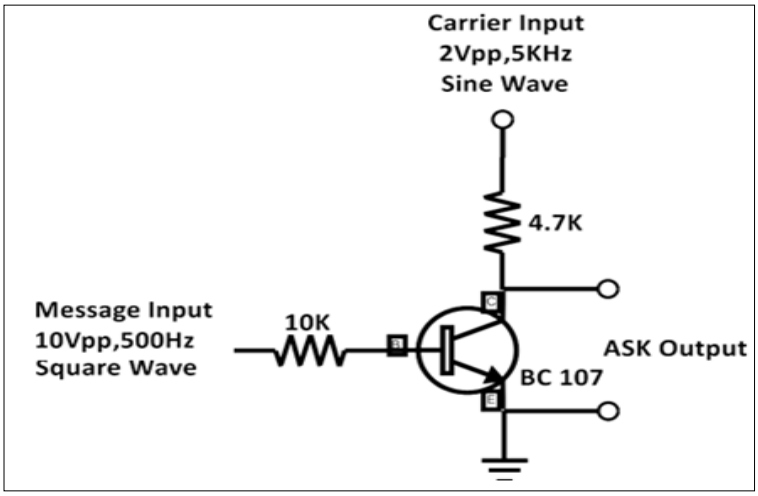
The demodulator circuit consists of an envelope detector and a comparator. The diode D selects the positive half cycle of the ASK input. The envelop detector formed by 2.2K resistor and 0.01uF capacitor detects the data out of the ASK input. The Op Amp comparator and the zener diode amplitude limiter convert this detected signal to its original logic levels. The 10K

potentiometer may be varied to set suitable reference voltage for the comparator.

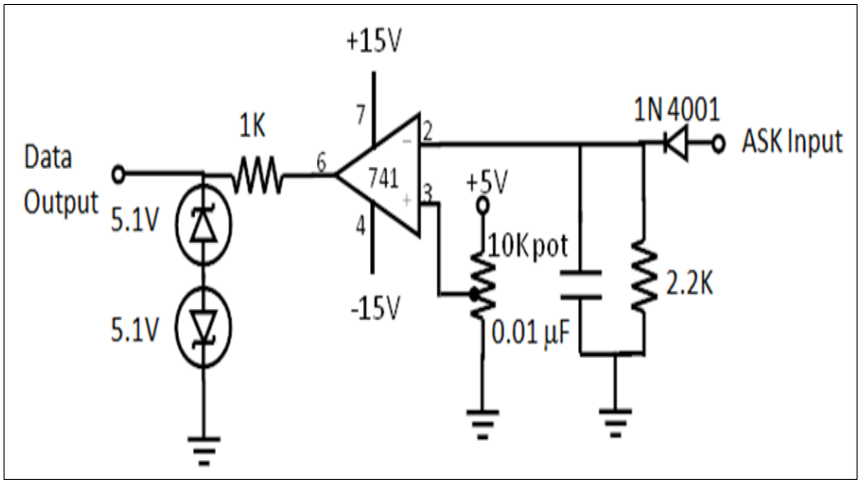
PROCEDURE:

1. Test all the components, bread board and probes.
2. Set up the circuits as shown in figure on the bread board.
3. Feed 10Vpp, 500Hz square wave as the message/data input and 2Vpp, 5KHz sine wave as the carrier input.
4. Observe both the message input and ASK output simultaneously on CRO and plot.
5. Apply the ASK output of the modulator to the demodulator input.
6. Observe both the ASK input and the demodulated output simultaneously on CRO. Adjust the reference voltage of the comparator if needed.
7. Plot the waveforms.

CIRCUIT DIAGRAM:

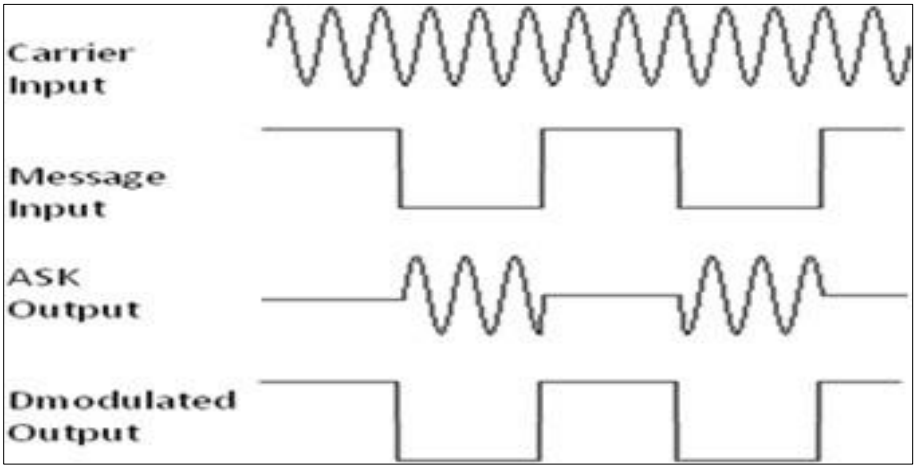


ASK Modulator



ASK Demodulator

WAVEFORMS:



RESULT:

ASK modulator and demodulator circuits were set up and the waveforms were plotted.

INFERENCE: Studied the simplest digital modulation scheme.

Experiment No.5

FREQUENCY SHIFT KEYING

AIM:

To set up FSK modulator and demodulator circuits and to observe the waveforms.

OBJECTIVES:

After completing this experiment, the students will be able to a) Set up FSK modulator and demodulator circuits and b) Identify FSK waveform.

COMPONENTS AND EQUIPMENTS REQUIRED:

Sl. No.	Item & Specification	Quantity
1	Transistor- BC 177	1No.
2	Resistor- 47K, 47K pot, 10K pot 10K	1No. each 7Nos.
3	Capacitor- 0.01μF 0.02μF 0.047μF, 0.001μF	3Nos. 4Nos. 1No.each
4	IC LM311	1No.
5	IC 555, IC 565	1No. each
6	Signal Generator	1Nos.
7	CRO	1No.
8	Power Supply- +/- 5V	1No.
9	Bread Board	1No.
10	Wires and probes	

THEORY:

Frequency Shift Keying (FSK) is a digital modulation scheme where the digital data is transmitted using a high frequency carrier signal. For logic '0' and '1' the carrier signal switches between two preset frequencies, hence the name FSK.

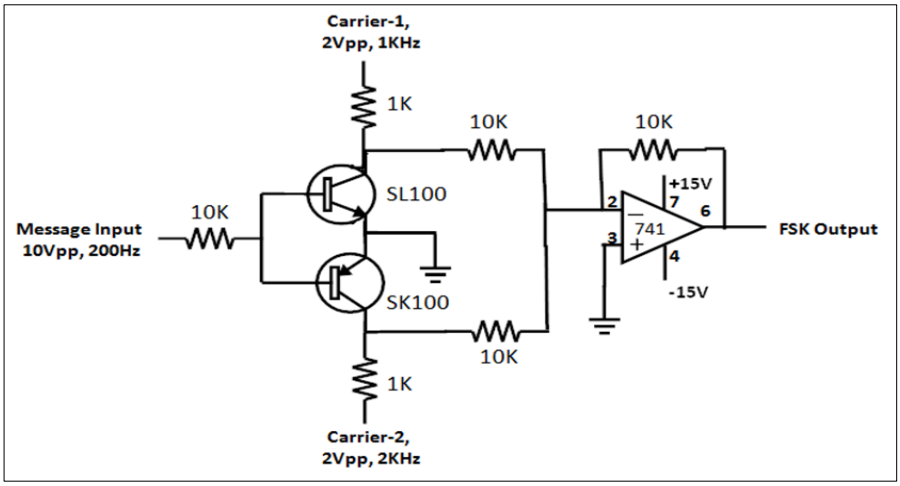
For logic '1' transistor SK100 is OFF and SL 100 is ON and vice versa, at any one time one frequency will be the output of the op-amp. Thus the output signal switches between the two preset frequencies for logic '0' and logic '1'. The resulting signal is FSK modulated.

PROCEDURE:

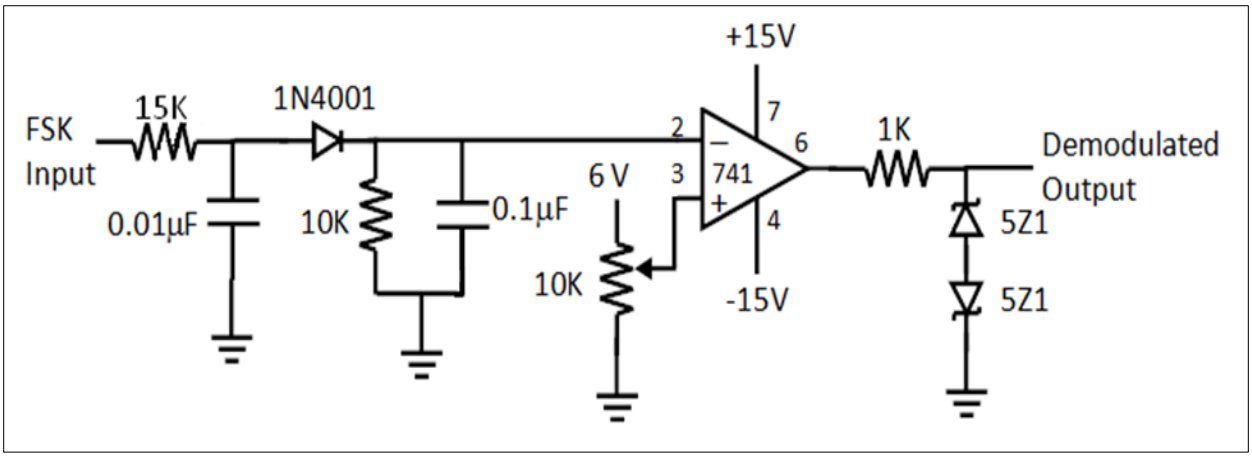
1. Test all the components and probes.
2. Set up the FSK modulator and demodulator circuits on the bread board. Switch on the power supplies.
3. Feed 5V, 100Hz (10Vpp, 100Hz) square wave as the data input. Vary the pot R_C to adjust the output frequencies if needed.
4. Observe both the input and output waveforms on CRO and plot. The waveform of the FSK output will be rectangular in nature for 555 modulator.

5. Apply the FSK output of the modulator to the input of the demodulator, and observe the output. Vary the 10K pot to get the PLL locked with the input signal. Plot the waveforms.

CIRCUIT DIAGRAM:

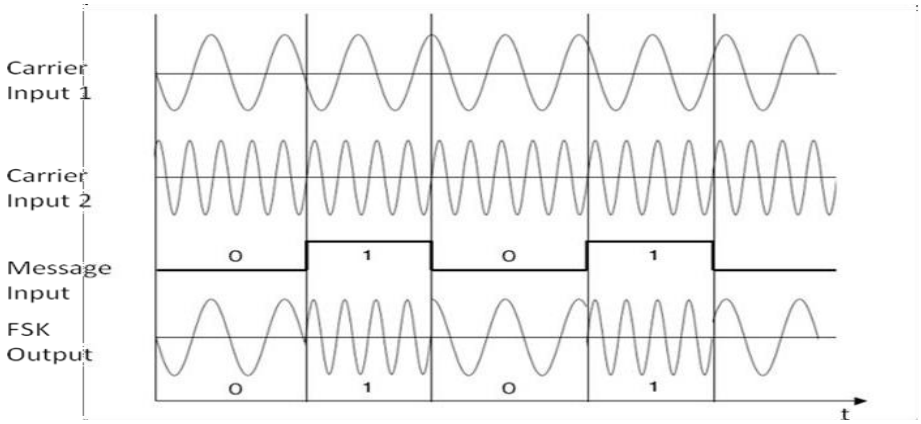


FSK Modulator



FSK Demodulator

WAVEFORM:



RESULT: The FSK modulator and demodulator circuits were set up and the waveforms were plotted.

Experiment No.6

BINARY PHASE SHIFT KEYING

AIM: To set up Binary Phase Shift Keying (BPSK) modulator and demodulator circuits and to observe the waveforms.

OBJECTIVES: After completing this experiment, the students will be able to a) Set up BPSK modulator and demodulator circuits and b) Identify BPSK waveform.

COMPONENTS AND EQUIPMENTS REQUIRED:

Sl. No.	Item & Specification	Quantity
1	Transistor- SL100, SK100	1No. each
2	Resistor- 10K pot, 100K 1K 10K	1No. each 3No. 7Nos.
3	Capacitor- 0.01μF	1No.
4	IC 741	3No.
5	Diode- 1N4001 Zener Diode- 5Z1	1No. 2Nos.
6	Signal Generator	2Nos.
7	CRO	1No.
8	Power Supply- +/- 15V, 2V	1No.each
9	Bread Board	1No.
10	Wires and probes	

THEORY:

Binary Phase Shift Keying (BPSK) is digital transmission scheme where the binary data is transmitted using out of phase signals. During logic '0' a preset number of cycles of a sinusoidal carrier signal is transmitted and during logic '1' the same number of cycles of the carrier signal is transmitted but with 180^o phase shift.

Modulator

A simple BPSK modulator circuit using an NPN-PNP transistor pair and an Op amp is shown in figure. The transistors work as switches and the Op amp works as inverting/non-inverting amplifier. The carrier signal is fed to the collectors and the message signal is fed to the bases of the two transistors simultaneously. The emitters of the transistors are grounded. When the message signal is at logic '1' (+5V), the NPN transistor is ON and works as a closed switch. The PNP transistor is OFF and works as an open switch. The Op amp now works as a non-inverting amplifier with the carrier signal fed to its non-inverting input. The carrier signal reaches the output without any phase shift. When the message signal is at logic '0' (-5V), the NPN transistor is OFF and the PNP transistor ON. The Op amp works as an inverting amplifier with the carrier signal fed to its inverting pin. The carrier signal now reaches the output with

180^o phase shift. Thus the carrier signal switches its phase as the message signal switches between '0' and '1'. The resulting output is BPSK modulated.

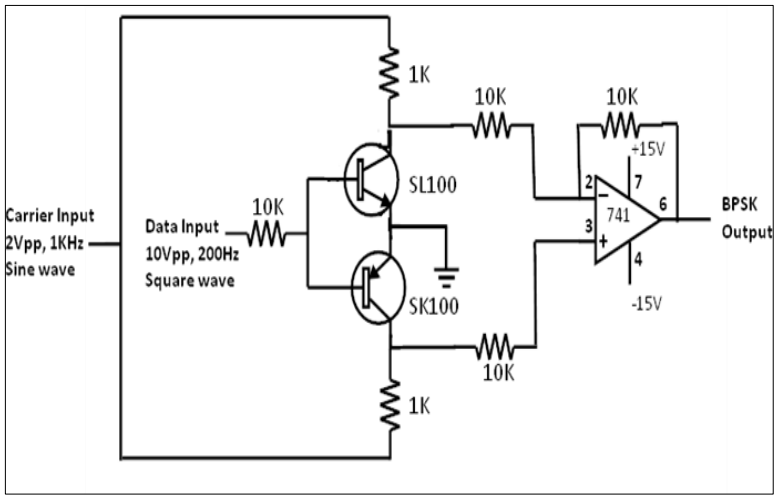
Demodulator

The BPSK demodulator circuit shown in figure consists of an Op Amp difference amplifier, a rectifier, an envelope detector and a comparator. The difference amplifier which is fed with the unmodulated carrier signal at the non-inverting input and the BPSK modulated signal at the inverting input passes only the phase shifted signal to the output. The in phase signals get subtracted completely. The envelope detector removes the carrier content and recovers the data information. The comparator inverts and level limits the signal to regain the correct logic level.

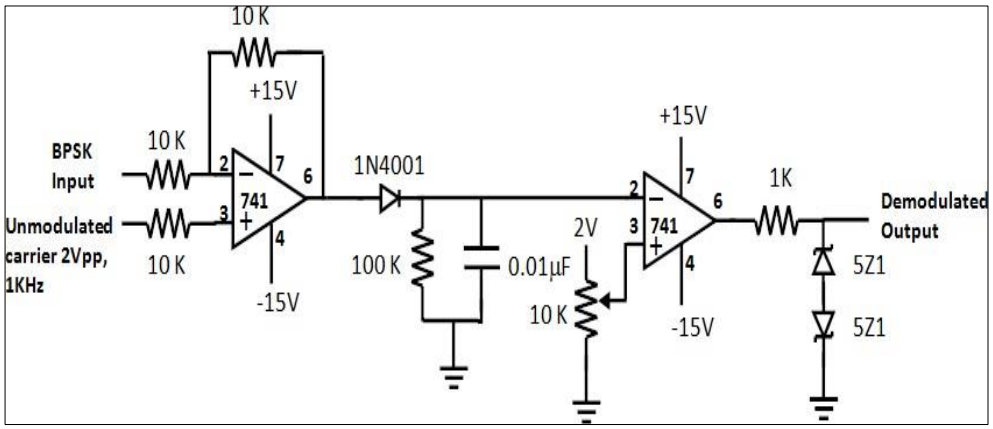
PROCEDURE:

1. Test all the components and probes.
2. Set up the circuits on the bread board as shown in figure.
3. Feed 2Vpp, 1KHz sine wave as carrier input and 10Vpp, 200Hz square wave signal as the message input.
4. Observe the BPSK output on CRO and plot the waveforms.
5. Feed this BPSK modulated signal to the inverting input of the demodulator. Also feed the unmodulated carrier signal (2Vpp, 1KHz) to the non-inverting input.
6. Observe waveforms on CRO. Adjust the potentiometer to obtain the correct output (if needed).
7. Plot the waveforms.

CIRCUIT DIAGRAM:

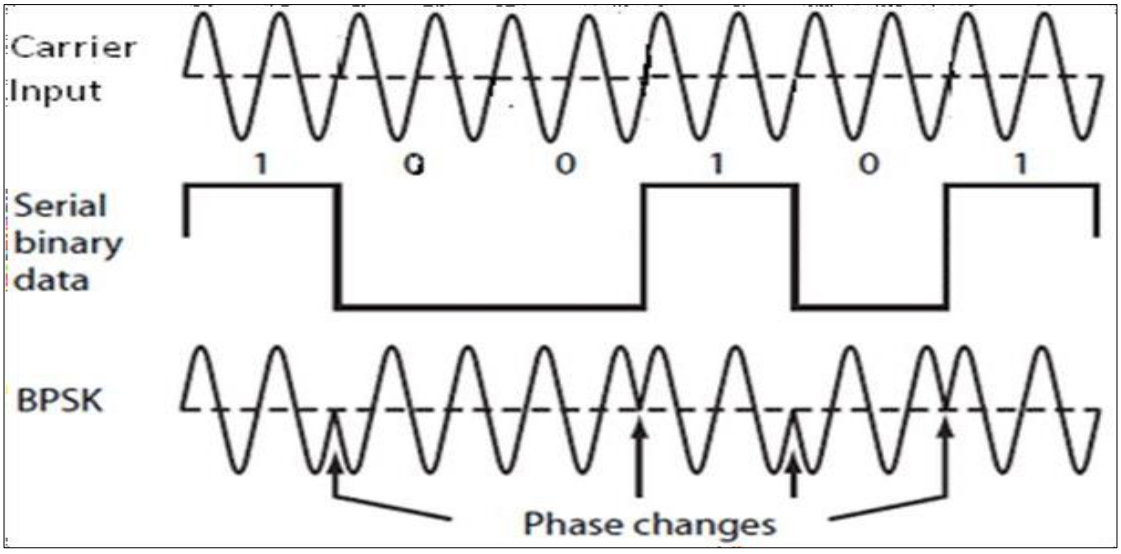


BPSK Modulator



BPSK Demodulator

WAVEFORMS:



RESULT:

BPSK modulator and demodulator circuits were set up and the waveforms were plotted.

INFERENCE: Studied how digital data is transmitted using BPSK.

Experiment No.7

TIME DIVISION MULTIPLEXER AND DEMULTIPLEXER

AIM:

To set up Time Division Multiplexer and Demultiplexer circuits and to observe the waveforms.

OBJECTIVES:

After completing this experiment, the students will be able to a) Set up TDM multiplexer and demultiplexer circuits.

COMPONENTS AND EQUIPMENTS REQUIRED:

Sl. No.	Item & Specification	Quantity
1	Transistor- SL100, SK100	1No. each
2	Resistor- 1K 10K	7Nos. 4Nos.
3	Capacitor- 1μF	2No.
4	IC 741	1No.
5	Signal Generator	3Nos.
6	CRO	1No.
7	Power Supply- +/- 15V	1No.
8	Bread Board	1No.
9	Wires and probes	

THEORY:

Time Division Multiplexing (TDM) is widely used in digital communication networks to transmit multiple signals simultaneously through the same channel. Different signals are transmitted in a time shared manner. Each signal is allotted a fixed time slot and a sample of the corresponding signal is transmitted during that period. After one sample each of all the signals is sent, the time slot is given back to the first signal and this process repeats.

TDM Multiplexer

A simple TDM multiplexer circuit using an NPN-PNP transistor pair and an Op amp is shown in figure. The transistors work as switches and the Op amp works as an adder. The signals to be sent are fed to the collectors of the two transistors. The switching signal is applied to the bases the transistors. During the ON time of the switching signal, the NPN transistor is ON and the PNP transistor is OFF. Signal 1 alone is connected to the adder input and reaches the output. During OFF time of the switching signal, the NPN transistor is OFF and the PNP transistor is ON. Signal 2 alone is connected to the adder input and reaches the output. Thus the two signals reach the output one after the other as the switching signal changes state. The resulting signal is a time division multiplexed one. The on-off period of the switching signal decides the time slot.

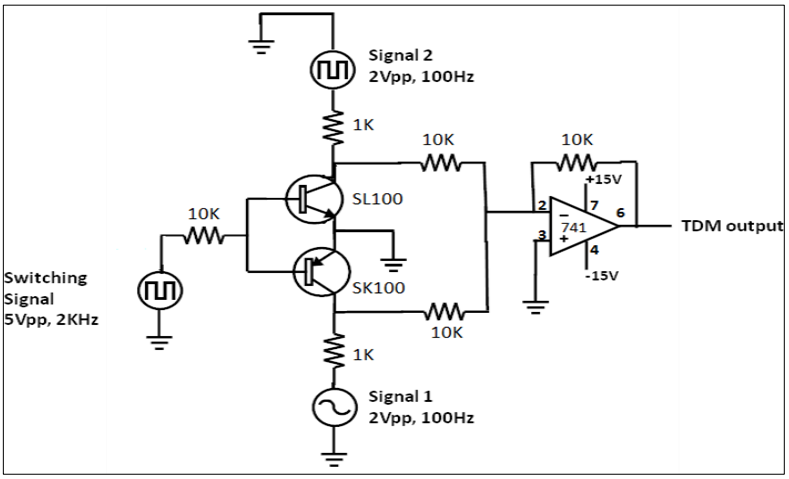
TDM Demultiplexer

In the demodulator circuit the two transistors act as switches. They connect the input TDM signal to the respective outputs alternately as the switching signal changes state. A square wave signal with the same phase and frequency as the one used at the TDM modulator is used as the switching signal. During the ON time of the switching signal, the NPN transistor is ON and the PNP transistor is OFF. TDM input is now connected to signal 1 output. During the OFF time of the switching signal, the NPN transistor is OFF and the PNP transistor is ON. TDM input is now connected to signal 2 output. The RC networks act as low pass filters.

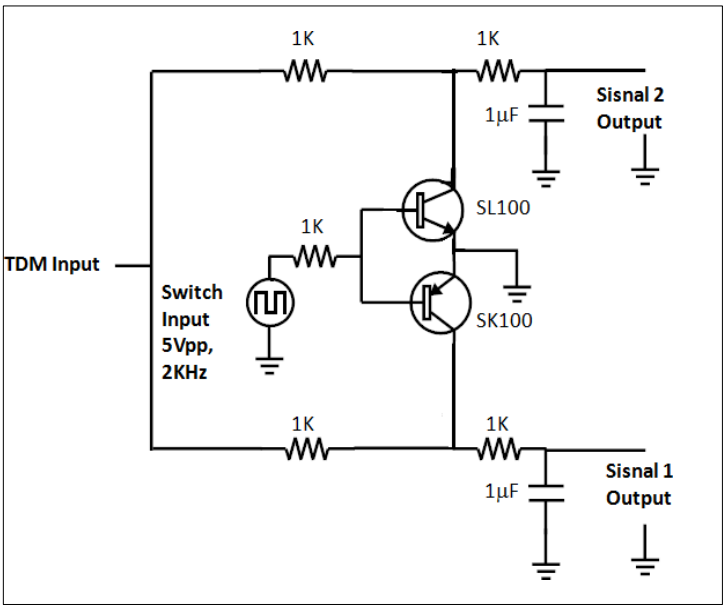
PROCEDURE:

1. Test all the components and probes.
2. Set up the circuits on the bread board as shown in figure.
3. Connect 5Vpp, 2KHz square wave signal as the switching input.
4. Connect 2Vpp, 100Hz sine wave as signal 1 and 2Vpp, 100Hz square wave as signal 2.
5. Observe the TDM output on CRO and plot the waveforms.
6. Feed this TDM output to the input of the demultiplexer. Use the same square wave signal used at the modulator as the switching signal.
7. Observe signal 1 and signal 2 outputs of the demultiplexer on CRO.
8. Plot the waveforms.

CIRCUIT DIAGRAM:

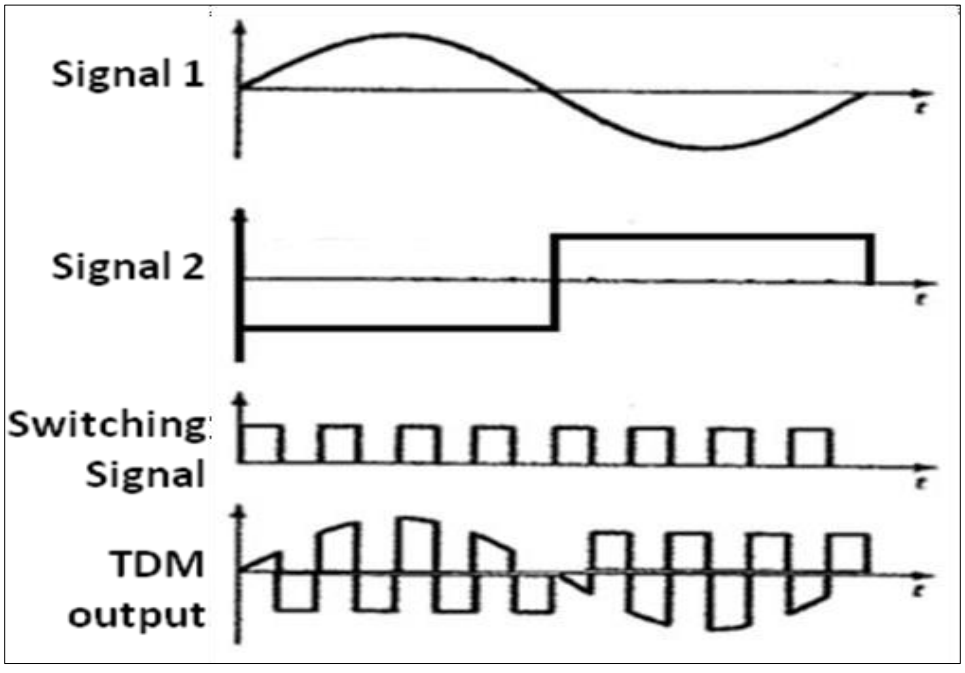


TDM Multiplexer



TDM Demultiplexer

WAVEFORM:



RESULT:

TDM Multiplexer and demultiplexer circuits were set up and the waveforms were plotted.

INFERENCE: Learned the basic idea of TDM multiplexing and demultiplexing.

Note: The demultiplexed outputs should be perfect sine and square waves. But with the given demultiplexer, the signal 2 output won't be a perfect square wave. An Op Amp comparator can be employed to make the output a perfect square wave.

Experiment NO 8, 9, and 10 experiments are performed using matlab simulation and Experiments No 11 and 12 are conducted using to OFC kit & Microwave setup.