JSS MAHAVIDYAPEETHA
JSS SCIENCE AND TECHNOLOGY UNIVERSITY
SRI JAYACHAMARAJENDRA COLLEGE OF ENGINEERING
- Constituent College of JSS Science and Technology University
- Approved by A.I.C.T.E
- Governed by the Grant-in-Aid Rules of Government of Karnataka
- Identified as lead institution for World Bank Assistance under TEQIP Scheme

JSS MAHAVIDYAPEETHA

JSS SCIENCE & TECHNOLOGY UNIVERSITY, MYSURU

ANALOG ELECTRONIC CIRCUITS - 20EC330L

LAB MANUAL

For 3rd Semester B.E Degree

Lab Location: AB201

Lab Incharge

Halesh M R, Asst. Professor.

Roopa M , Asst. Professor.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

2021-2022

Vision of the Institute

1. **Advancing JSS S&T University as a leader in education, research and technology on the international arena.**
2. **To provide the students a universal platform to launch their careers, vesting the industry and research community with skilled and professional workforce.**
3. **Accomplishing JSS S&T University as an epicentre for innovation, centre of excellence for research with state of the art lab facilities.**
4. **Fostering an erudite, professional forum for researchers and industrialist to coexist and to work cohesively for the growth and development of science and technology for betterment of society.**

Mission of the Institute

1. **Education, research and social outreach are the core doctrines of JSS S&T University that are responsible for accomplishment of in-depth knowledge base, professional skill and innovative technologies required to improve the socio economic conditions of the country.**
2. **Our mission is to develop JSS S&T University as a global destination for cohesive learning of engineering, science and management which are strongly supported with interdisciplinary research and academia.**
3. **JSS S&T University is committed to provide world class amenities, infrastructural and technical support to the students, staff, researchers and industrial partners to promote and protect innovations and technologies through patents and to enrich entrepreneurial endeavors.**
4. **JSS S&T University core mission is to create knowledge led economy through appropriate technologies, and to resolve societal problems by educational empowerment and ethics for better living.**

Vision statement of the department

Be a leader in providing globally acceptable education in electronics and communication engineering with emphasis on fundamentals-to-applications, creative-thinking, research and career-building.

Mission statement of the department

1. **To provide best infrastructure and up-to-date curriculum with a conducive learning environment.**
2. **To enable students to keep pace with emerging trends in Electronics and CommunicationEngineering.**
3. **To establish strong industry participation and encourage student entrepreneurship.**
4. **To promote socially relevant eco-friendly technologies and inculcate inclusive innovation activities.**

Program Educational Objectives (PEOs) of the Department

1. **To enable the graduates to have strong Engineering fundamentals in Electronics & Communication, with adequate orientation to mathematics and basic sciences.**
2. **To empower graduates to formulate, analyze, design and provide innovative solutions in Electronics and Communication, for real life problems.**
3. **To ensure that graduates have adequate exposure to research and emerging technologies through industry interaction and to inculcate professional and ethical values.**
4. **To nurture required skill sets to enable graduates to pursue successful professional career in industry, higher education, competitive exams and entrepreneurship.**

CYCLE OF EXPERIMENTS

CYCLE – I: For Event 2	**PART - A**
1.	Clippers and Clampers Circuits.
2.	Rectifiers.
3.	BJT characteristics.
4.	MOSFET characteristics.
5.	Frequency response of single stage RC–Coupled Amplifier.
CYCLE II: For Event 4	**PART - B**
6.	RC– Low pass and High Pass filters.
7.	BJT Darlington Emitter follower circuit.
8.	Voltage series feed-back amplifier.
9.	Negative Feed-back amplifier.
10.	Oscillators.

JSS MAHAVIDYAPEETHA: JSS SCIENCE AND TECHNOLOGY UNIVERSITY (FORMERLY SJCE)

RECORD OF PERFORMANCE IN THE LAB CLASS FOR CIE

Section		**Batch**		**Group Number**	
Staff in Charge		**Day**		**Timings**	

Sl. No.	**USN**	**Name Of The Student**	**AC1: Preparedness (8M)** **AC2: Conduction (8M)** **AC3: Viva (8M)** **AC4: Report Writing (8M)** **AC5: Result Interpretation (8M)** **T: Total (40M)**	**SUBJECT:** **Analog Electronic Circuits Lab** **20EC330**
1.				
2.				
3.				
4.				

PART - A

Date	**Experiment**	**Student-1**						**Student-2**						**Student-3**						**Student-4**					
		AC 1	**AC 2**	**AC 3**	**AC 4**	**AC 5**	**T**	**AC 1**	**AC 2**	**AC 3**	**AC 4**	**AC 5**	**T**	**AC 1**	**AC 2**	**AC 3**	**AC 4**	**AC 5**	**T**	**AC 1**	**AC 2**	**AC 3**	**AC 4**	**AC 5**	**T**
	Introduction to Lab and components	**Not to be evaluated**																							
	Clippers and Clampers Circuits																								
	Rectifiers																								
	BJT characteristics																								
	MOSFET characteristics																								
	Frequency response of single stage RC–Coupled Amplifier																								
	Event – 2: Simulation of Part A Experiments evaluated for 40 Marks																								

PART - B

Date	Experiment	Student-1						Student-2						Student-3						Student-4					
		AC 1	AC 2	AC 3	AC 4	AC 5	T	AC 1	AC 2	AC 3	AC 4	AC 5	T	AC 1	AC 2	AC 3	AC 4	AC 5	T	AC 1	AC 2	AC 3	AC 4	AC 5	T
	RC– Low pass and High Pass filters																								
	BJT Darlington Emitter follower circuit																								
	Voltage series feedback amplifier																								
	Negative Feedback amplifier																								
	Oscillators																								
	Event – 4: Test will be conducted for 40 Marks																								
Event – 2 (20 Marks) Average of Part A experiments and simulations marks reduce to 20 Marks																									
Event – 4 (20 Marks) Average of Part B experiments and Test marks reduce to 20 Marks																									

INTRODUCTION

OVERVIEW OF ANALOG ELECTRONIC CIRCUITS LABORATORY

Analog Electronics as the name suggests deals mainly with processing of Analog signals. Analog electronic circuit design is one of the important and challenging field in Electronics. The area of analog electronics is one of the vast and complex areas in VLSI circuits design. A signal which is having different values at different instants of time and having its value defined at every instants of time is referred to as an analog signal. Circuits to process analog signals are necessary because all the naturally available signals like human speech, sound ,biomedical, temperature etc are analog in nature. Analog electronic circuits can be designed and tested for their performance using the CAD tools like PSPICE, Cadence, etc.. Many analog circuits are available in the form of IC chips.

During this Lab course simple analog electronic circuits are designed using discrete components like Resistors, Capacitors, Inductors, PN junction diodes and Transistors (BJT's, FET's, etc.). These designed circuits are tested and verified for their performance under the laboratory conditions using power sources like DC Power supply, AC sources like function generators. Their input and output parameters like input waveforms, output waveforms, input and output current and voltage readings, the impedance or resistance offered by the circuit, etc are analyzed by using measuring instruments like multi-meter and CRO's. The captured values from the instruments are noted and used for further calculations.

Similar to Analog electronics, we have Digital electronics which mainly deals with digital circuit design. A Digital signal can be represented by using only two values 0 or 1 at any instant of time. Logic gates, Flip-Flops, Registers, etc are some examples of basic digital circuits. Digital circuits are mainly classified as Combinational and Sequential circuits. The experiments on these circuits will be dealt in logic design laboratory.

All the signals are basically analog signals. So there exists need for converting an Analog signal to a Digital signal or vice versa. Analog to Digital converters (ADC's) and Digital to Analog converters (DAC's) with different specifications are available for this purpose. Digital signal processing is fast compared to the processing of analog signals. So in most of the applications the input analog information is converted to its digital equivalent and there after the digital equivalent of the analog signal is processed. It is again converted back to its analog form to retrieve the original analog signal. A simple and popular example is MP3 format representation of the audio signals which are basically analog in nature, i.e. the audio or speech signals. Both analog and digital electronics play an important role in the field of – Electronics and communications.

Digital electronics field is like a catalyst for processing analog signals with desired and designed levels of accuracy.

ANALOG ELECTRONICS LABORATORY COURSE FLOW:

This laboratory course completely deals with basics of analog electronic circuit design and their experimental observations. Here the students are exposed to design and implement the analog circuits like Clipping and Clamping circuits using diodes, Amplifiers using FET's or BJT's, verification of circuit theorems such as Thevenin's and maximum power transfer theorems, behavior of RL, RLC circuits, oscillators such as RC phase shift, Hartley, Colpitt's and Crystal oscillators, full wave and half wave rectifier circuits, resonance circuits, etc..

To start with this laboratory session, initially all students are trained to use the measuring instruments like Multi-meter and CRO. Thorough understanding of CRO is mandatory for proceeding with the course wear. The function or signal generators which generate the analog signals of desired frequency and amplitude (frequency and voltage levels) are made familiar to the students. Reading the values of the passive components like resistor, capacitor, etc. using color code are taught.

After completing the above exercise, the design aspects of analog circuits are carried out. Thereafter the conduction of the experiments are started to verify and test the performance of the designed analog circuits. The input and generated output waveforms are sketched and the results are noted for further calculations.

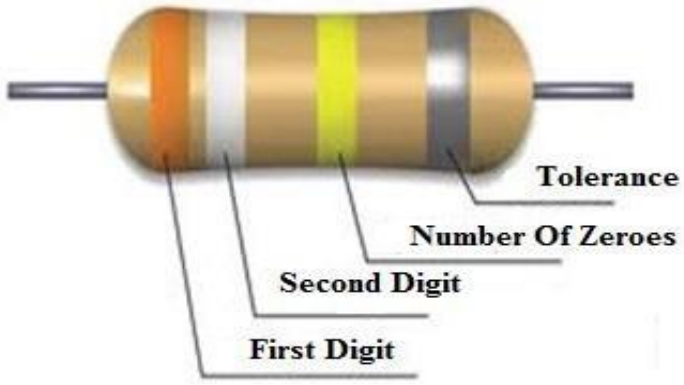
Instructions to the students are given in the start of this document which they are advised to read before they start conducting experiments.

INSTRUCTIONS BEFORE STARTING THE EXPERIMENT

1. Study the circuit, theory and procedures, expected output before doing the experiment.
2. Get familiarize with the components and equipments used in the lab, Ex: Resistors, Capacitors Inductors, Signal generators, BJTs, FETs, CROs, Digital Multi-meter etc.

3. RESISTORS

The Resistors used in this lab are of two types, (1) fixed value resistors which havecolour bands and (2) Variable value resistors (Decade Resistance Box(DRBs)).



Digit	Colour
0	Black
1	Brown
2	Red
3	Orange
4	Yellow
5	Green
6	Blue
7	Violet
8	Grey
9	White
Tolerance	**Colour**
20%	No Band
10%	Silver
5%	Gold

Fig 1. A fixed value resistor **Table 1. Colours with Digits**

A Fixed value resistor looks as shown in the above image. The value of this kind of resistors is determined as shown below.

We have to start from the side opposite to the gold or silver colour and go left to right. Now the

Value of Resistor=(First colour digit)(Second colour digit)(That many zeroes as third colour digit) ±

(Fourth colour) ohms

=(First Digit)(Second Digit)(Number of Zeroes) ± (Tolerance) Ω

For example ,if for a given resistor ,first colour is **Brown** ,second colour is **White**, third colour **Yellow** and fourth colour is **Silver**, then the value of this resistor is determined using Table 1 and above equation as,

Value of resistor =(First Digit)(Second Digit)(Number of Zeroes) ±(Tolerance) Ω

= (1) (9) (0000) ± 10%

= 190000 ± 0.1

≈190 KΩ (neglecting tolerance)

Note : Finding the value of a variable value resistor (DRB) is straight forward in which we will set the value using knobs provided on the DRBs. The value of the resistor is sum of the values shown by each knob.

4. CAPACITORS

Fig 2 . Ceramic Capacitor

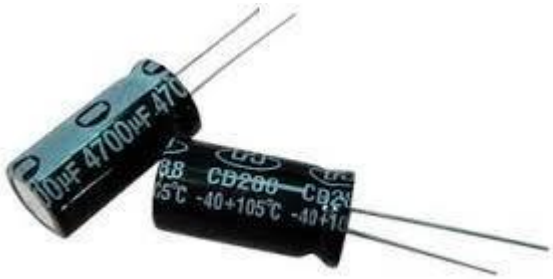


Fig 3. Electrolytic Capacitor

Capacitors are of two types , (a) Ceramic capacitor and (b) Electrolytic capacitors .They look like as shown in Fig 1 and Fig 2 given above.

(a) Ceramic Capacitor : Ceramic capacitors have no polarity and the value of these capacitors is

determined by using the digits shown on their body in fig 2, as follows ,

Value of capacitor= (First two digits)(That many Zeroes as third digit) pico farads

For example. if the digits shown on the capacitor is **154** , then its value is determined as ,

Value of capacitor = (First two digits)(That many Zeroes as third digit) pico farads

= (15) (0000) pF

$=150000 \times 10^{-12}$ F (since $pF=10^{-12}$ F)

$=15 \times 10^{4} \times 10^{-12}$ F

$=15 \times 10^{-8} = 0.15 \times 10^{-6} =$ **0.15 uF**

(b) Electrolytic Capacitor : Electrolytic Capacitors have polarities ,so their terminals are represented as positive and negative terminals that we can identify by seeing the body of

the capacitor that appears as shown in Fig 2 given above. Usually the lengthier terminal is the positive terminal and shorter terminal is the negative terminal. The value of the capacitor is given on the body of the capacitor itself.

5. SIGNAL GENERATOR AND ITS ADJUSTMENTS

Signal generator or Function generator is an electronic instrument which is used as AC signal source to give AC input signals of different shapes (square wave ,sine wave ,etc) and wide range of frequency required by the circuit. It has Voltage and Frequency knobs to adjust Voltage and Frequency of the input AC signals.

Fig 4. Signal or Function generator

Before connecting the signal generator to the circuit check the followings

a. Set the shape of the waveform (sinusoidal).

b. Set the frequency using coarse and fine adjustments.

c. Set the offset adjustments. Set the CRO in DC mode and ensure the waveform is symmetry in both positive and negative cycle. If not , adjust it using the DC offsetting potentiometer

d. Set the Voltage magnitude using Vcoarse settings and Vfine adjustments.

6. CRO (CATHODE RAY OSCILLOSCOPE) AND ITS ADJUSTMENTS

CRO (Cathode Ray Oscilloscope) is an electronic instrument used to display ,observe and analyse the outputs of the circuits. It has two channels two display two different outputs. Each channel has two axis ,vertical axis which represents amplitude and horizontal axis which represents time. Values of amplitude and time of the signal are measured by using corresponding amplitude and time knob(which is common for both channels) on the CRO for both channels.

Fig 5. Cathode Ray Oscilloscope

a. Select the right voltage and time scale to get the proper waveform
b. For clipper and clamper circuits, observe the waveform in DC mode only
c. Set the input waveform mainly for offset setting in DC mode only.
d. Before measurement, ensure X & Y are in calibrated mode (if provided externally)
e. Ensure that Channel selection and trigger mode are properly set.
f. In case of two channels do not mix the signal and ground terminals.

7. MULTI-METER ADJUSTMENTS

Fig 6. Multi Meter

a. Set the right mode before taking the readings. Wrong mode settings may damage the instrument.

b. For current reading, connect the multi-meter in mA (or A) mode to the circuit before switching on the supply. Do not remove the current meter when the supply is on. Check for ac and dc modes as required.

c. Use the proper probes for the measurement. Wrong cables may damage the instrument.

8. IDENTIFICATION OF TRANSISTOR TERMINALS

Fig 7. Transistor

Hold the Transistor as shown in Fig 7 given above . From the notch or Tab in the anticlockwise direction, **first** is **Emitter** , **middle** one is **Base** and the last i.e. **third** terminal is **Collector** terminal.

9. VOLTAGE REGULATED POWER SUPPLY (VRPS) (Dual D.C Power Supply)

Fig 8. Voltage Regulated Power Supply

VRPS is used to provide D.C power required by the circuit if any and it looks as shown in Fig 8

10. BREAD BOARD

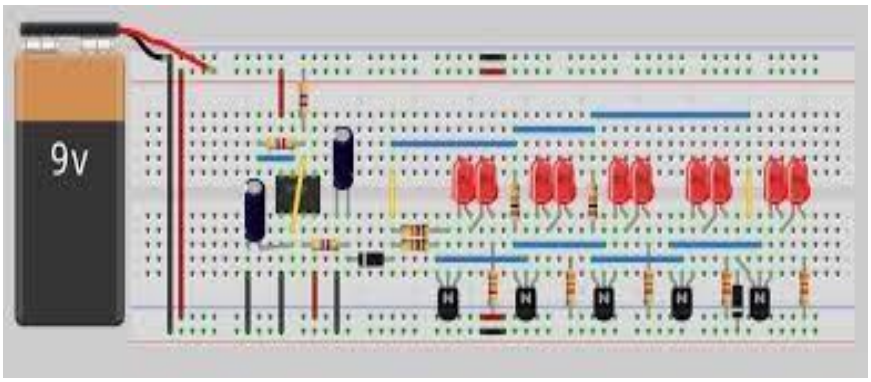


Fig 9. Bread Board

Bread Board is apparatus which is used as the base to connect components of the circuit as shown in the Fig 9. Bread Board has connections points which are divided into rows and columns which in turn are internally shorted.

11. After adjusting the input voltage, check the circuit connections before turning the power on.

12. The ground connections are made properly & ensure that the circuit has one ground.

13. Connect the ground terminal of signal generator and the oscilloscope to the same point. Do not mix the ground point and signal of the two instruments to get the proper readings.

14. Don't pull out the connections with the power supply on.

15. Use only stripper to remove insulation.

16. Don't short the terminals while checking the output at pin terminals.

17. Don't switch on supply to the circuit unless the staff has checked the circuit connections.

EXPERIMENT NO. 1A

CLIPPER CIRCUITS

AIM: Conduct experiment to test diode clipping (single/double ended).

COMPONENTS REQUIRED

Sl. No	APPARATURS AND COMPONENTS	Range	Quantity
01	Bread board		1
02	Diode	1N4007	2
03	Resistors	10KΩ	1
04	VRPS	0-30V DC, 3A	1
05	CRO for testing		1
06	Signal generator	10Hz to 1MHz	1
07	Probes, wires		1
08	Digital multimeter		1

THEORY

Clippers are networks that employ diodes to clip away portions of an input signal without distorting the remaining part of the applied waveform. These clipper circuits transfer a selected portion of the input waveform to the output Diode clipping circuits are used to prevent a wave form from exceeding some particular limit either negative or positive or both. This is achieved by connecting the diode in serial or in parallel circuit. Variable DC voltage is connected in the circuit to achieve required level of clipping. By using different level DC voltages, it is possible to get different level of clipping in positive and negative side. These clipper circuits are also called as limiters.

Following are few types of clipper circuits

1. Single ended (positive or negative) and double ended clipping

2. Series or parallel based on the construction.

Peak detection is possible by connecting a suitable capacitor across the output of single ended clipping circuit. The capacitor charging time to be fast and discharging time to be slow so that capacitor holds the maximum value.

1(A) SHUNT CLIPPERS (SINGLE ENDED CLIPPING)

1(A).1 CLIPPING ABOVE THE REFERENCE VOLTAGE(V_{ref})

CIRCUIT DIAGRAM

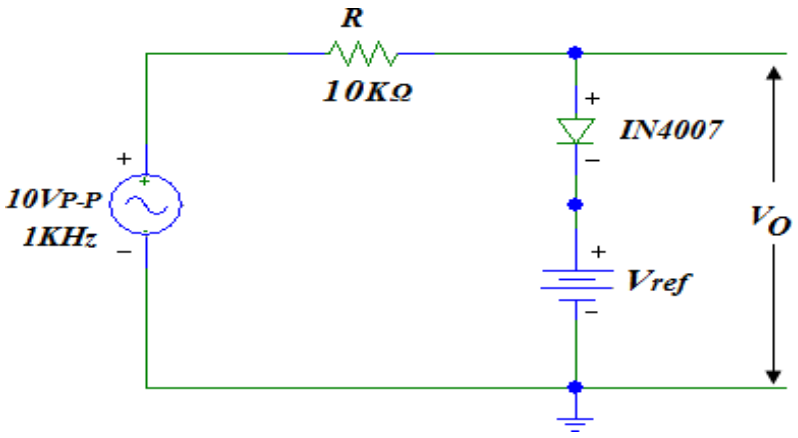


Fig 1(A).1.a Shunt clipper for clipping above the reference level.

DESIGN

Let the output voltage be clipped at say Vo= +4V

Therefore Vo(max)=+4V

From Fig 7(B).1.a above ,Vo(max)=V_γ + Vref (Where V_γ=V_K= cut in voltage of the diode≈0.6V)

Therefore Vref=Vo(max)- V_γ=4 – 0.6 =3.4V

The value of resistor R is designed usually by equation R=$\sqrt{RfRr}$

Where Rf= diode forward resistance = 10Ω

and Rr= diode reverse resistance = 10MΩ

Therefore R=$\sqrt{10 \times 10 \times 10^6}$ =10KΩ

PROCEDURE

1. Make the connections for the clipping circuit as shown in the Fig 6(A).1.a
2. Switch on the VRPS and set the supply voltage Vref=3.4V
3. Apply a Sine Wave input (Vin) at frequency say 1KHz from the Signal generator and adjust the Voltage to a peak to peak amplitude of say 10V(p-p) (peak amplitude should be greater than clipping level always otherwise clipping will not occur).
4. Observe the Input waveform , Output waveform and clipping level in CRO .
5. Apply Vin and Vo to the X and Y channels of CRO respectively and obtain the transfer characteristics using X-Y mode in CRO .

OUTPUT WAVEFORM

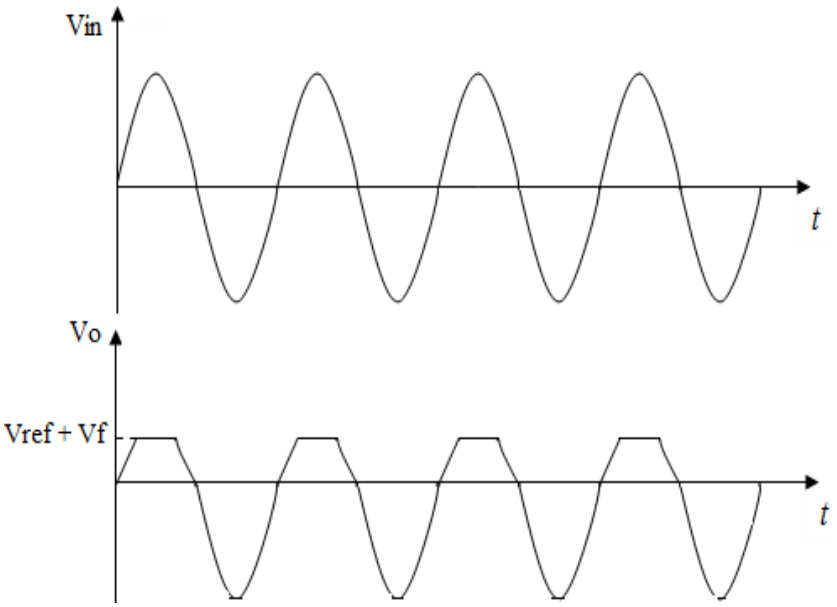


Fig 1(A).1.b Wave form of shunt clipper for clipping above reference level.

TRANSFER CHARACTERISTICS

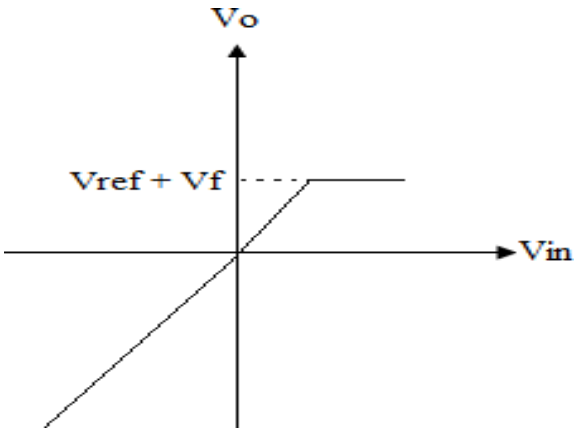


Fig 1(A).1.c Transfer characteristics of shunt clipper for clipping above reference level.

1(A).2 CLIPPING BELOW THE REFERENCE VOLTAGE(V_{ref})

CIRCUIT DIAGRAM

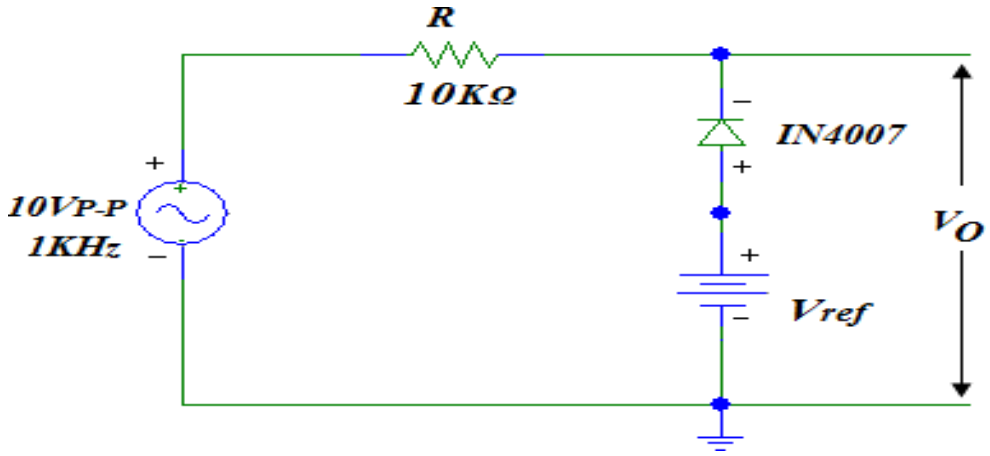


Fig 1(A).2.a Shunt clipper for clipping below the reference level.

DESIGN

Let the output voltage be clipped at say Vo= +4V

Therefore Vo(min)=+4V

From Fig 6(B).2.a above ,Vo(min)= $-V_\gamma$ + Vref (Where $V_\gamma=V_K$=Vf cut in voltage of the diode≈0.6V)

Therefore **Vref**=Vo(min) + V_γ=4 + 0.6 = **4.6V**

The value of resistor R is designed usually by equation R=$\sqrt{RfRr}$

Where Rf= diode forward resistance = 10Ω

and Rr= diode reverse resistance = 10MΩ

Therefore **R**=$\sqrt{10 \times 10 \times 10^6}$ =**10KΩ**

PROCEDURE

1. Make the connections for the clipping circuit as shown in the Fig 6(A).2.a
2. Switch on the VRPS and set the supply voltage Vref=4.6V
3. Apply a Sine Wave input (Vin) at frequency say 1KHz from the Signal generator and adjust the Voltage to a peak to peak amplitude of say 10V(p-p) (peak amplitude should be greater than clipping level always otherwise clipping will not occur).
4. Observe the Input waveform , Output waveform and clipping level in CRO .
5. Apply Vin and Vo to the X and Y channels of CRO respectively and obtain the transfer characteristics using X-Y mode in CRO .

OUTPUT WAVEFORM

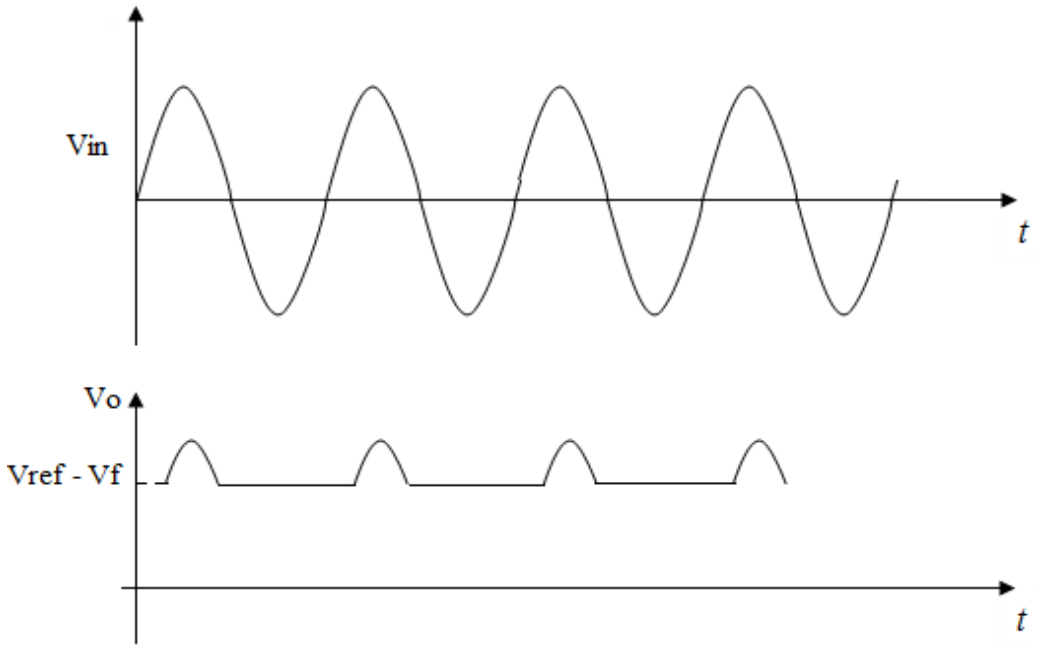


Fig 1(A).2.b Wave form of shunt clipper for clipping below reference level.

TRANSFER CHARACTERISTICS

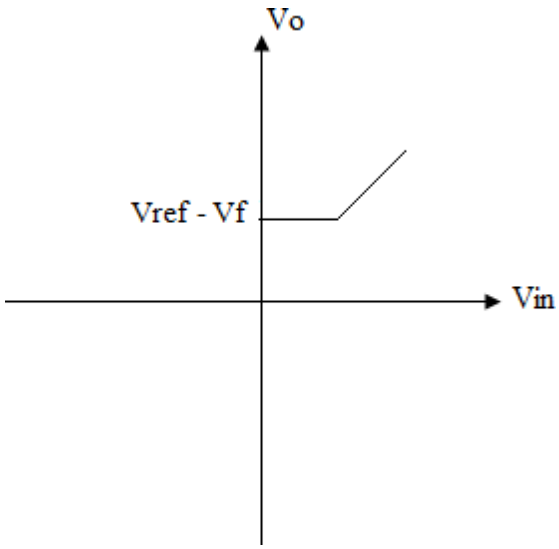


Fig 1(A).2.c Transfer characteristics of shunt clipper for clipping below reference level.

1(B) DOUBLE ENDED SHUNT CLIPPING CIRCUITS

1(B).1 CLIPPING AT TWO POSITIVE ENDS (ASYMMETRICAL CLIPPER)

CIRCUIT DIAGRAM

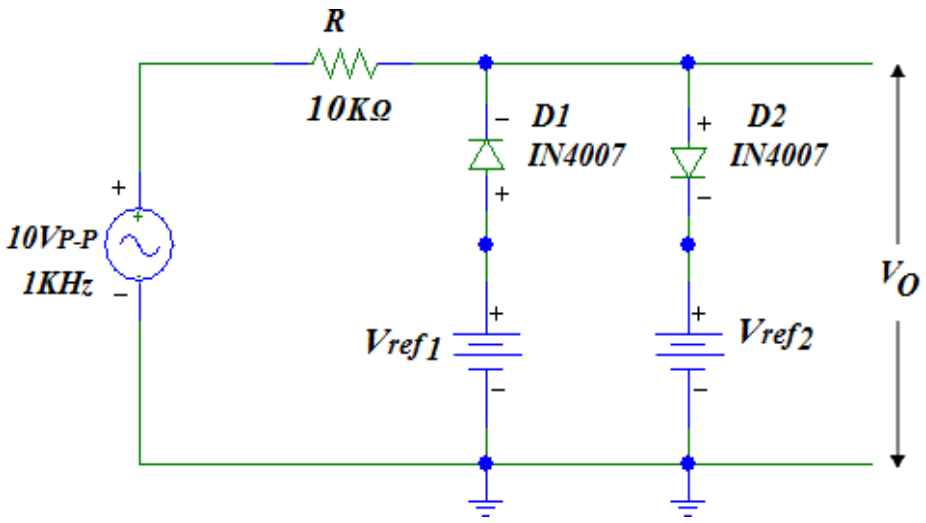


Fig 1(B).1.a Two level clipping circuit.

DESIGN

Let the output voltage be clipped at say Vo(max)= +6V and Vo(min)=+3V

Let Vref2 > Vref1

We have Vo(max)= 6V

We have from Fig 7(B).1.a above, Vo(max)=Vref2 + V_γ Where V_γ is diode D2 cut in voltage ≈ 0.6V

Therefore **Vref2**=Vo(max) - V_γ=6 - 0.6 = **5.4V**

Also we have Vo(min)= 3V

We have from Fig 7(B).1.a above, Vo(min)=Vref1 - V_γ Where V_γ is diode D2 cut in voltage ≈ 0.6V

Therefore **Vref1**=Vo(min) + V_γ=3 + 0.6 = **3.6V**

The value of resistor R is designed usually by equation R=$\sqrt{RfRr}$

Where Rf= diode forward resistance = 10**Ω**

and Rr= diode reverse resistance = 10M**Ω**

Therefore **R**=$\sqrt{10 \times 10 \times 10^6}$ =**10KΩ**

PROCEDURE

1. Make the connections for the clipping circuit as shown in the Fig 6(B).1.a
2. Switch on the VRPS and set the supply voltage Vref1=6.6V and Vref2=5.4V
3. Apply a Sine Wave input (Vin) at frequency say 1KHz from the Signal generator and adjust the Voltage to a peak to peak amplitude of say 10V(p-p) (peak amplitude should be greater than clipping level always otherwise clipping will not occur).
4. Observe the Input waveform , Output waveform and clipping level in CRO .
5. Apply Vin and Vo to the X and Y channels of CRO respectively and obtain the transfer characteristics using X-Y mode in CRO .

OUTPUT WAVEFORMS

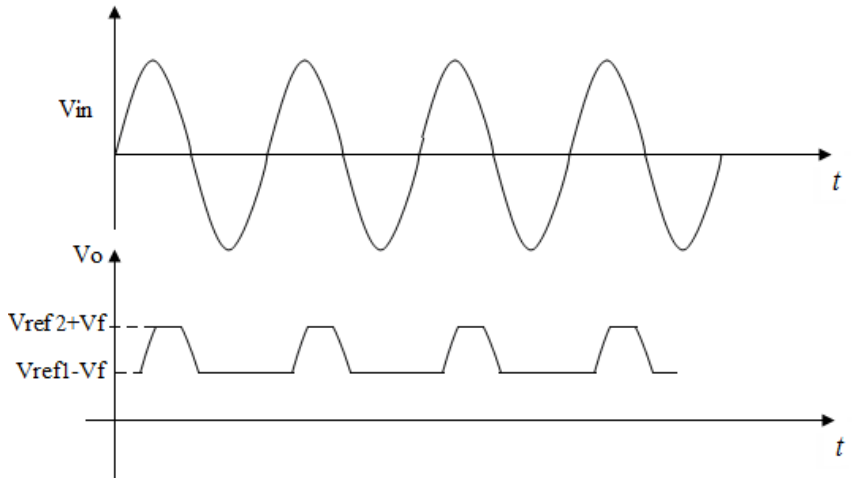


Fig 1(B).1.b Wave form of a Two level clipper.

TRANSFER CHARACTERISTICS

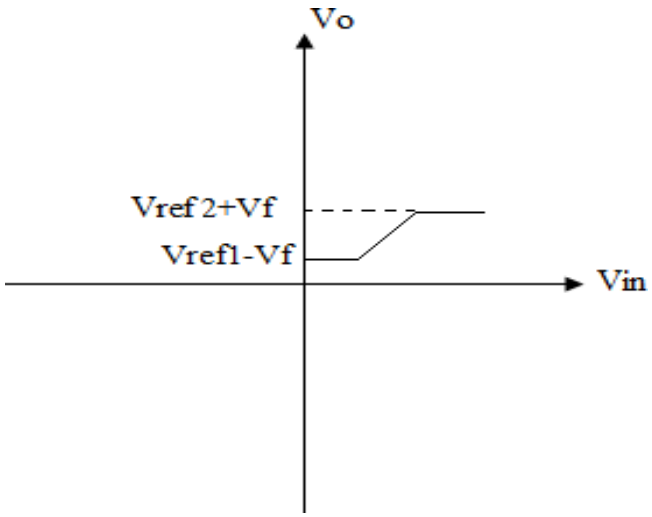


Fig 1(B).1.c Transfer characteristics of two level clipper.

1(B).2 CLIPPING AT TWO INDEPENDENT LEVELS (SYMMETRICAL CLIPPER)

CIRCUIT DIAGRAM

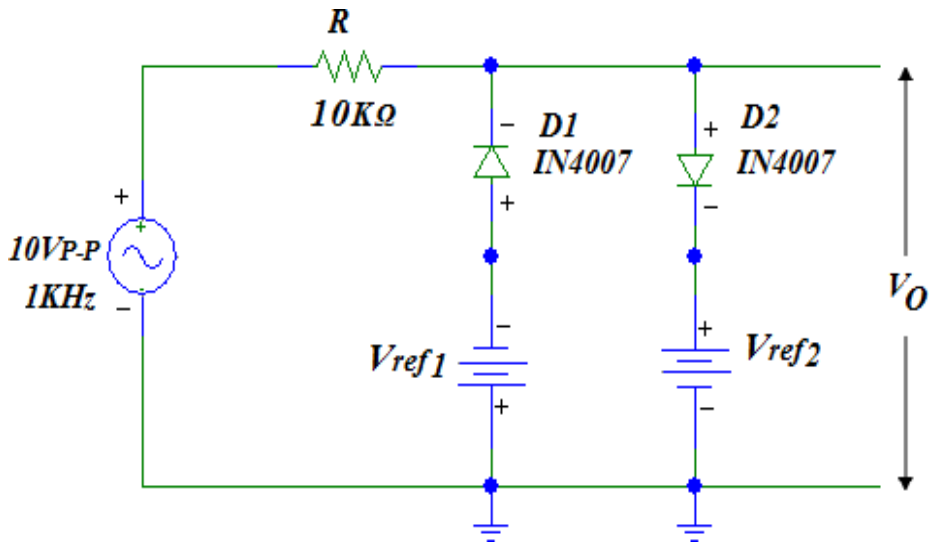


Fig 1(B).2.a Two level clipper to clip at two independent level.

DESIGN

Let the output voltage be clipped at say Vo(max)= +6V and Vo(min)=-6V

We have, Vo(max)= 6V

We have from Fig 7(B).2.a above, Vo(max)=Vref2 + V_γ Where V_γ is diode D2 cut in voltage ≈ 0.6V

Therefore **Vref2**=Vo(max) - V_γ=6 - 0.6 = **5.4V**

Also we have Vo(min)= -6V

We have from Fig 7(B).1.a above, Vo(min)=-Vref1 - V_γ Where V_γ is diode D2 cut in voltage ≈ 0.6V

Therefore **Vref1**= -Vo(min) + V_γ= -(-6) + 0.6 = **6.6 V**

The value of resistor R is designed usually by equation R=$\sqrt{RfRr}$

Where Rf= diode forward resistance = 10Ω

and Rr= diode reverse resistance = 10MΩ

Therefore **R**=$\sqrt{10 \times 10 \times 10^6}$ =**10KΩ**

PROCEDURE

1. Make the connections for the clipping circuit as shown in the Fig 6(B).2.a
2. Switch on the VRPS and set the supply voltage Vref1=-5.4V and Vref2=5.4V
3. Apply a Sine Wave input (Vin) at frequency say 1KHz from the Signal generator and adjust the Voltage to a peak to peak amplitude of say 10V(p-p) (peak amplitude should be greater than clipping level always otherwise clipping will not occur).
4. Observe the Input waveform , Output waveform and clipping level in CRO .
5. Apply Vin and Vo to the X and Y channels of CRO respectively and obtain the transfer characteristics using X-Y mode in CRO .

OUTPUT WAVEFORM

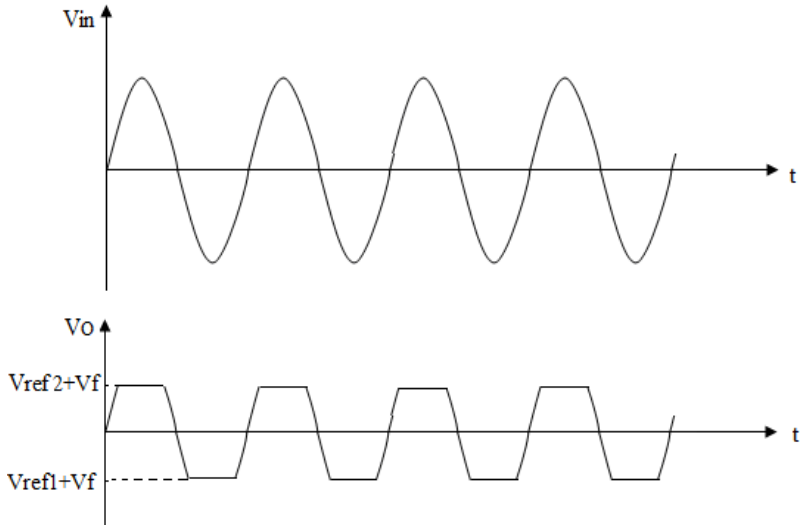


Fig 1(B).2.b wave form of two level clipper to clip at two independent level

TRANSFER CHARACTERISTICS

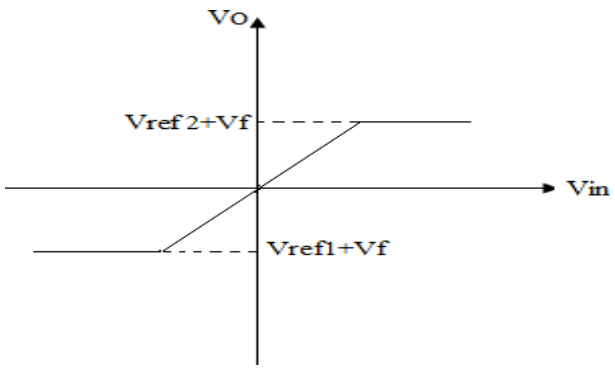


Fig 1(B).2.c Transfer characteristics of two level clipper to clip at two independent level.

RESULT: Diode Clipper Circuits designed and verified with different configurations.

EXPECTED VIVA QUESTIONS

1. What is Semiconductor?
2. What is Intrinsic Semiconductor?
3. What is extrinsic Semiconductor?
4. What is p-n junction?
5. What is doping?
6. What is knee voltage?
7. What is breakdown voltage?
8. What is peak inverse voltage (PIV) of diode?
9. What is the maximum power rating?
10. What is the drift current?
11. What is diffusion current?.
12. What is diffusion capacitance?
13. In what condition of the diode diffusion capacitance occurs?
14. What is diode?
15. What are the characteristics of ideal diode, when it is forward bias?
16. What are the characteristics of ideal diode when it is reverse biased?

OBSERVATION AND WORK SHEET

GRAPH SHEETs HAVE TO BE INSERTED

EXPERIMENT NO. 2

DIODE CLAMPING CIRCUITS.

AIM

To Design and Verify positive and negative clamping circuits.

COMPONENTS REQUIRED

Sl. No	APPARATURS AND COMPONENTS	Range	Quantity
01	Bread board		1
02	Diode	1N4007	2
03	Capacitor	0.1μ F	1
04	VRPS	0-30Vdc 3A	1
05	CRO for testing		1
06	Probes, wires		1
07	Digital multimeter		1

THEORY

Clamper is a circuit that "clamps" a signal to a different DC level without changing the appearance (or Shape) of the applied signal. The different types of clampers are positive , negative and biased clampers. A clamping network must have a capacitor, a diode and a resistive element. The magnitude of R and C must be chosen such that the time constant RC is large enough to ensure that the voltage across the capacitor does not discharge significantly during the interval the diode is not conducting. By connecting suitable DC voltage in series with the diode, the level of swing can be varied.

A circuit that places either the Positive or Negative peak of a signal at a desired fixed DC level is known as clamping circuit. A clamping circuit essentially adds DC to the input A.C signal. In positive clamper the input signal is a square wave having a peak value of V (volts). The clamper adds the DC component and pushes the signal upwards so that the negative peaks fall on the zero level. It may be seen that the shape of the original signal has not changed, only there is vertical shift in the signal .Such a clamper is called a positive clamper. The negative clamper does the reverse that is it pushes the signal downwards so that positive peak falls on the zero level. A clamping circuit should not change peak to peak value of the signal. It should only change the DC level. To do so, a clamping circuit uses a capacitor, together with a diode and a load resistor R_L.

The operation of a clamper is based on the principle that charging time of a capacitor is made very small as compared to its discharging time.

2(A) POSITIVE CLAMPING CIRCUIT WITH REFERENCE VOLTAGE (Vref)

OR NEGATIVE PEAK CLAMPER WITH REFERENCE VOLTAGE(Vref)

CIRCUIT DIAGRAM

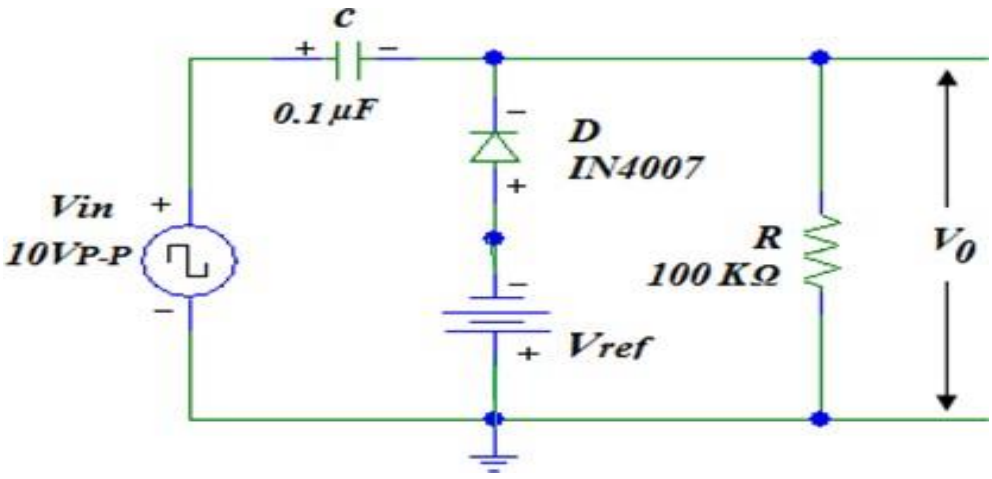


Fig 2(A).a Positive clamper with Vref

DESIGN

Let negative peak be clamped at Vo(min)=-4V

From Fig given above , Vo(min)=-Vref - V_γ

Therefore Vref=-Vo(min) - V_γ =-(-4) – 0.6 = 3.4V

Let input frequency = 1KHz .Therefore T= 1 / f = 1 ms.

Let RC=10T (because discharge time of the capacitor should be >> T)

Let R=100KΩ , therefore C=10 ms / 100KΩ= 0.1uF.

So use R=100KΩ and C=0.1uF.

PROCEDURE

1. Rig up the circuit as shown in the circuit diagram.
2. Set the input to 10V(p-p) square wave.
3. Select the input signal Vin amplitude to 10V(p-p) and 1kHz frequency .

4. Observe and verify the output waveform.

INPUT AND OUTPUT WAVEFORMS

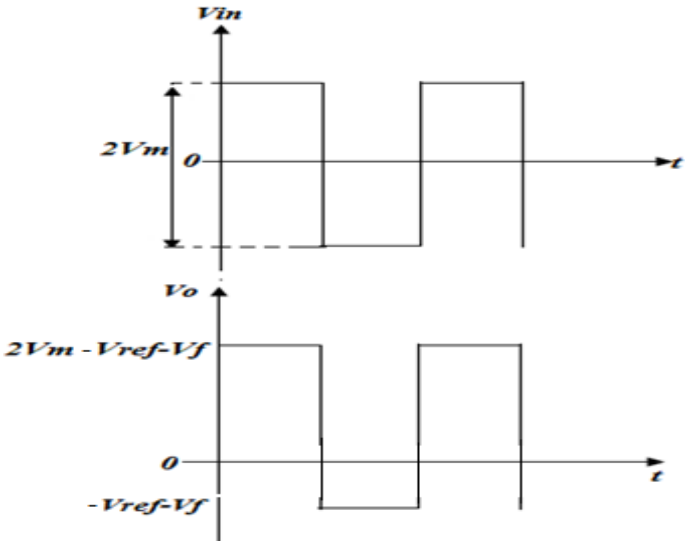


Fig.2(A).b Waveforms of positive clamper with Vref

2(B) NEGATIVE CLAMPING CIRCUIT WITH REFERENCE VOLTAGE(Vref)

OR POSITIVE PEAK CLAMPER WITH REFERENCE VOLTAGE(Vref)

CIRCUIT DIAGRAM

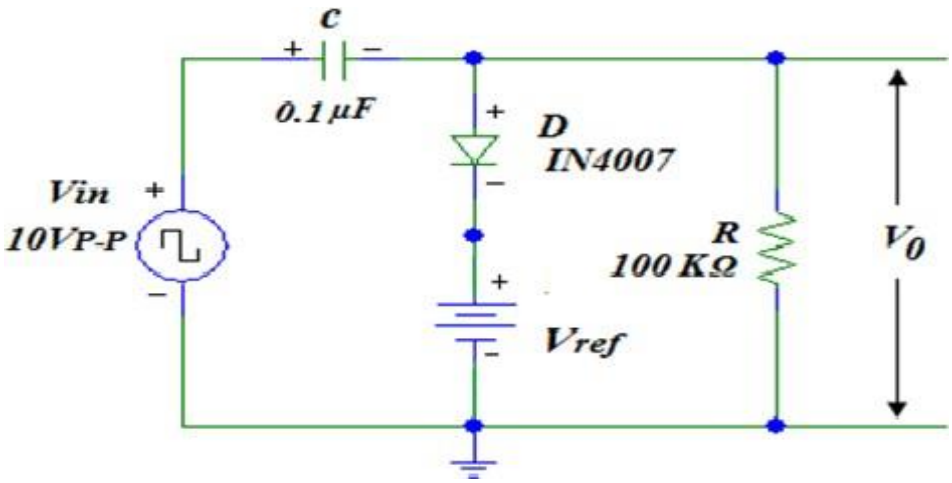


Fig 2(B).a Negative clamper with Vref

DESIGN

Let positive peak be clamped at Vo(max)=+4V

From Fig given above , Vo(max)=Vref + V_γ

Therefore Vref=Vo(max) - V_γ =4 – 0.6 =3.4V

Let input frequency = 1KHz .Therefore T= 1 / f = 1 ms.

Let RC=10T (because discharge time of the capacitor should be >> T)

Let R=100KΩ , therefore C=10 ms / 100KΩ= 0.1uF.

So use R=100KΩ and C=0.1uF.

PROCEDURE

1. Rig up the circuit as shown in the circuit diagram.
2. Set the input to 10V(p-p) square wave.
3. Select the input signal Vin amplitude to 10V(p-p) and 1kHz frequency.
4. Observe and verify the output waveform.

INPUT AND OUTPUT WAVEFORMS

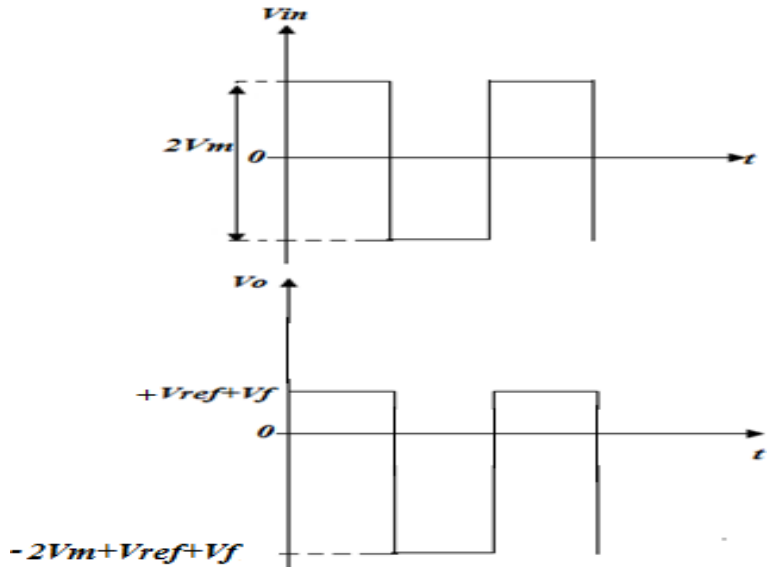


Fig.2(B).b Waveforms of negative clamper with Vref

RESULT

Both the positive and negative clamping circuits are designed and observed the variation in the swing as DC voltage varies.

EXPECTED VIVA QUESTIONS

1. What is Semiconductor?
2. What is anIntrinsic Semiconductor?
3. What is an extrinsic Semiconductor?
4. What is a p-n junction?
5. What is doping?
6. What is the knee voltage of a diode?
7. What is breakdown voltage?
8. What is peak inverse voltage (PIV) of a diode?
9. What is the maximum power rating a diode?
10. What is drift current?
11. What is diffusion current?.
12. What is diffusion capacitance?
13. In what condition of the diode diffusion capacitance occurs?
14. What is a diode? What the name diode stands for?
15. What are the characteristics of an ideal diode when it is forward biased?
16. What are the characteristics of an ideal diode when it is reverse biased?
17. Define clamping.
18. Mention different types of clamping circuits.
19. What are the applications of clamping circuits?

OBSERVATION AND WORK SHEET

GRAPH SHEETs HAS TO BE INSERTED

EXPERIMENT NO. 2A

HALF -WAVE RECTIFIER WITH AND WITHOUT FILTER

AIM: To examine the input and output waveforms of half wave Rectifier and also Calculate its load regulation and ripple factor.

1. With Filter.
2. Without Filter

COMPONENTS REQUIRED

Sl. No	APPARATURS AND COMPONENTS	Range	Quantity
01	Bread board		1
02	Diode	1N4007	2
03	Decade Resistance Box	10KΩ	1
04	Transformer	6V-0-6V	1
05	CRO for testing		1
06	Signal generator	10Hz to 1MHz	1
07	Probes, wires		1
08	Digital multimeter		1
09	Capacitor	100μf/470 μf	1

THEORY

In Half Wave Rectification, When AC supply is applied at the input, only Positive Half Cycle appears across the load whereas, the negative Half Cycle is suppressed. How this can be explained as follows:

During positive half-cycle of the input voltage, the diode D1 is in forward bias and conducts through the load resistor R_L. Hence the current produces an output voltage across the load resistor R_L, which has the same shape as the +ve half cycle of the input voltage.

During the negative half-cycle of the input voltage, the diode is reverse biased and there is no current through the circuit. i.e., the voltage across R_L is zero. The net result is that only the +ve half cycle of the input voltage appears across the load. The average value of the half wave rectified o/p voltage is the value measured on dc voltmeter.

For practical circuits, transformer coupling is usually provided for two reasons.

1. The voltage can be stepped-up or stepped-down, as needed.
2. The ac source is electrically isolated from the rectifier. Thus preventing shockhazards in the

secondary circuit.

The efficiency of the Half Wave Rectifier is 40.6%

Theoretical calculations for Ripple factor:

Without Filter*:*

Vrms = Vm/2

Vm = 2Vrms

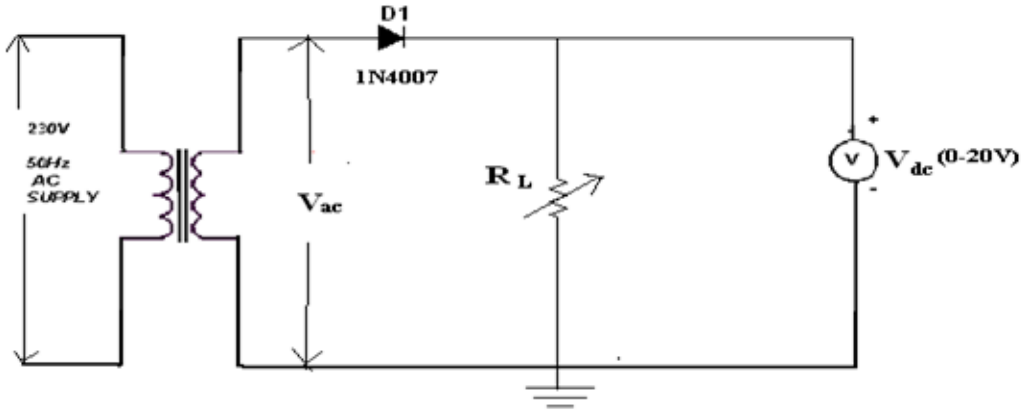
Vdc = Vm/Π

Ripple factor $r=\sqrt{(Vrms/Vdc)^2 - 1} = 1.21$

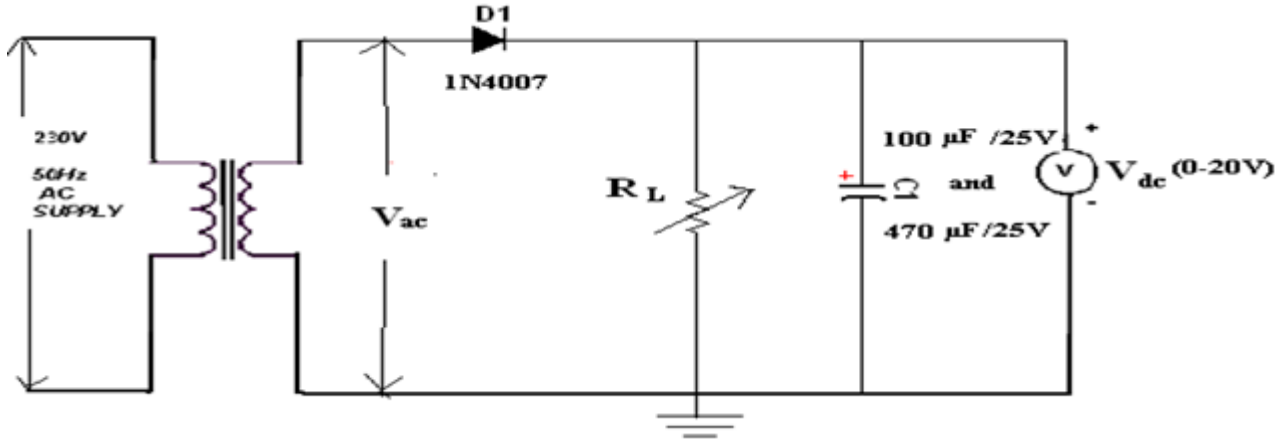
With Filter*:* Ripple factor, $r = 1/(2\sqrt{3}\, f C R)$

CIRCUIT DIAGRAM:

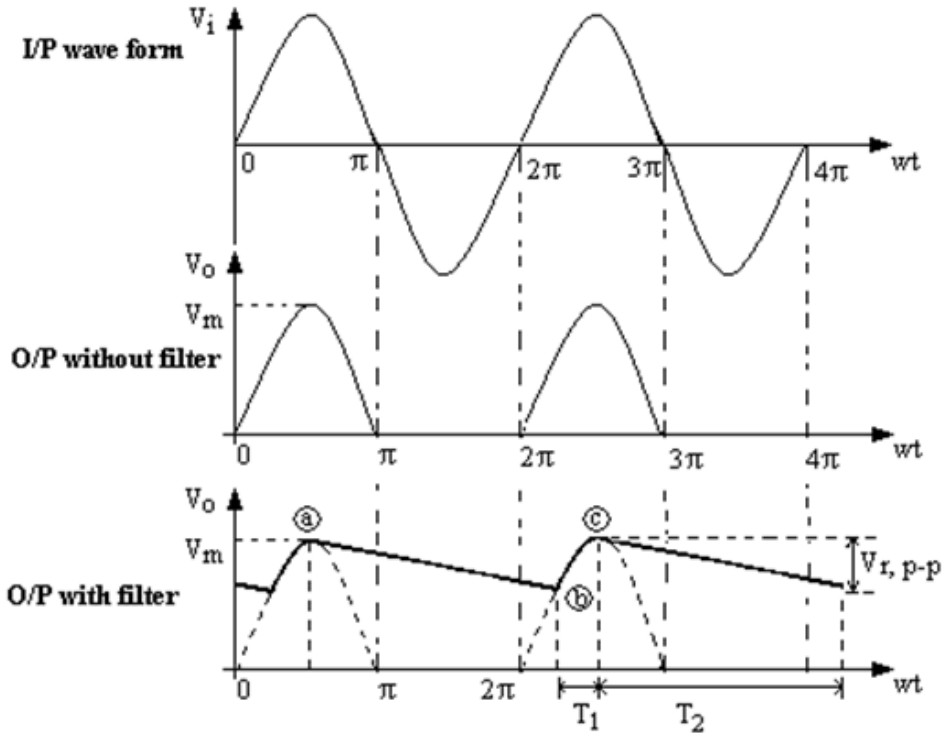
A) Half Wave Rectifier without Filter:



B) Half Wave Rectifier with Filter:



Waveforms



Half-wave Rectifier with capacitor filter wave form

PROCEDURE:

1. Connections are made as per the circuit diagram.
2. Connect the primary side of the transformer to ac mains and the secondary side to therectifier input.
3. By the multimeter, measure the ac input voltage of the rectifier and, ac and dc voltageat the output of the rectifier.
4. Find the theoretical value of dc voltage by using the formula, Vdc=Vm/Π
   Where, Vm=2Vrms, (Vrms=output ac voltage.)
5. The Ripple factor is calculated by using the formula
   r = ac output voltage/dc output voltage.

Without Filter:

V no load Voltage (Vdc) = V

S.No	Load Resistance R_L kilo-ohms	O/P Voltage (Vo) V_{ac} (V)	O/P Voltage (Vo) V_{dc} (V)	Ripple factor $\left(\gamma = \frac{V_{ac}}{V_{dc}}\right)$	% of Regulation $\left(\frac{V_{NL} - V_{FL}}{V_{NL}} * 100\%\right)$
1	1				
2	2				
3	3				
4	4				
5	5				
6	6				
7	7				
8	8				
	.				

WITH CAPACITOR FILTER:

V no load Voltage (Vdc) = V

S.No	Load Resistance R_L kilo-ohms	O/P Voltage (Vo) V_{ac} (V)	O/P Voltage (Vo) V_{dc} (V)	Ripple factor $\left(\gamma = \frac{V_{ac}}{V_{dc}}\right)$	% of Regulation $\left(\frac{V_{NL}-V_{FL}}{V_{NL}} * 100\%\right)$
1	1				
2	2				
3	3				
4	4				
5	5				
6	6				
7	7				
8	8				

REGULATION CHARACTERSTICS:

1. Connections are made as per the circuit diagram.
2. By increasing the value of the rheostat, the voltage across the load and currentflowing through the load are measured.
3. The reading is tabulated.
4. From the value of no-load voltages, the %regulation is calculated using theformula,

%Regulation = $[(V_{NL}-V_{FL}) /V_{FL}]*100$

PRECAUTIONS:

1. The primary and secondary side of the transformer should be carefully identified
2. The polarities of all the diodes should be carefully identified.
3. While determining the % regulation, first full load should be applied and then it should be decremented in steps

RESULT:

VIVA QUESTIONS:

1. What is the PIV of Half wave rectifier?
2. What is the efficiency of half wave rectifier?
3. What is the rectifier?
4. What is the difference between the half wave rectifier and Full Wave Rectifier?
5. What is the o/p frequency of Bridge Rectifier?
6. What are the ripples?
7. What is the function of the filters?
8. What is TUF?
9. What is the average value of o/p voltage for HWR?
10. What is the peak factor?

EXPERIMENT NO. 2B

FULL-WAVE RECTIFIER WITH AND WITHOUTFILTER

AIM: To Examine the input and output waveforms of Full Wave Rectifier and also calculate its load regulation and ripple factor.

1. With Filter
2. Without Filter

COMPONENTS REQUIRED

Sl. No	APPARATURS AND COMPONENTS	Range	Quantity
01	Bread board		1
02	Diode	1N4007	2
03	Decade Resistance Box	10KΩ	1
04	Transformer	6V-0-6V	1
05	CRO for testing		1
06	Signal generator	10Hz to 1MHz	1
07	Probes, wires		1
08	Digital multimeter		1
09	Capacitor	100μf/470 μf	1

THEORY:

The circuit of a center-tapped full wave rectifier uses two diodes D1&D2.

During positive half cycle of secondary voltage (input voltage), the diode D1 is forward biased and D2 is reverse biased. So the diode D1 conducts and current flows through load resistor RL.

During negative half cycle, diode D2 becomes forward biased and D1 reverse biased. Now, D2 conducts and current flows through the load resistor RL in the same direction. There is a continuous current flow through the load resistor RL, during both the half cycles and will get unidirectional current as show in the model graph. The difference between full wave and half wave rectification is that a full wave rectifier allows unidirectional (one way) current to the load during the entire 360 degrees of the input signal and half-wave rectifier allows this only during one half cycle (180 degree).

THEORITICAL CALCULATIONS:

Vrms = Vm/ √2

Vm = Vrms√2

Vdc = 2Vm/Π

(i) Without filter:

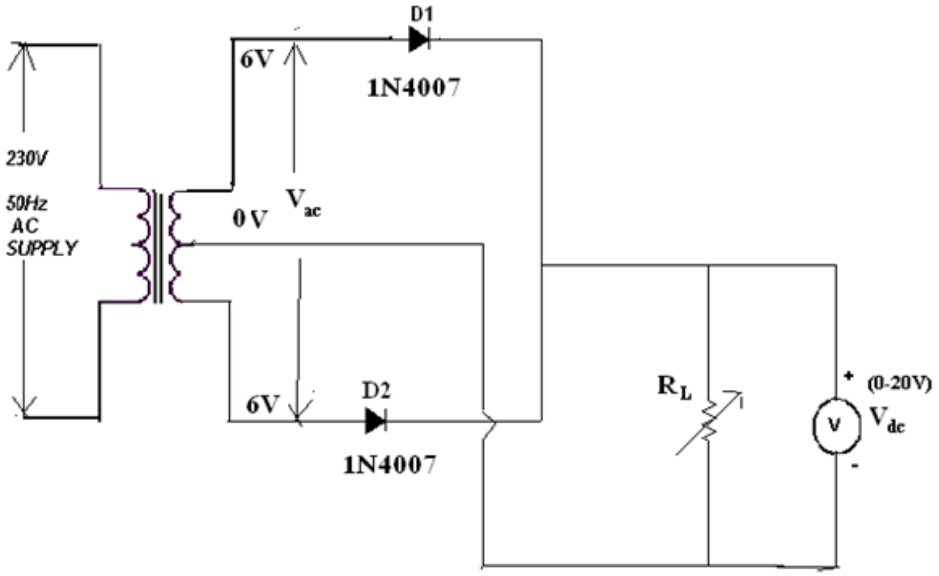
Ripple factor, r = √ (Vrms/ Vdc)2 -1 = 0.812

(ii) With filter:

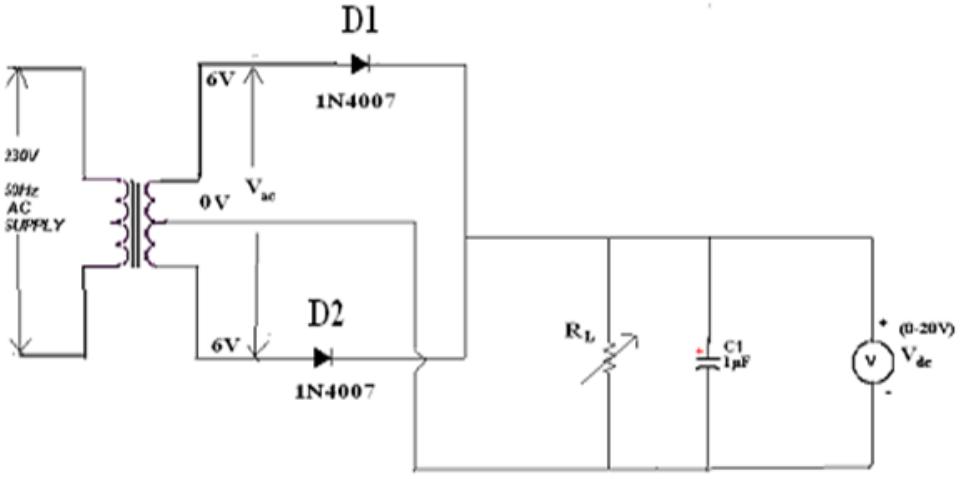
Ripple factor, r = 1/ (4√3 f C RL)

CIRCUIT DIAGRAM:

A) FULL WAVE RECTIFIER WITHOUT FILTER:

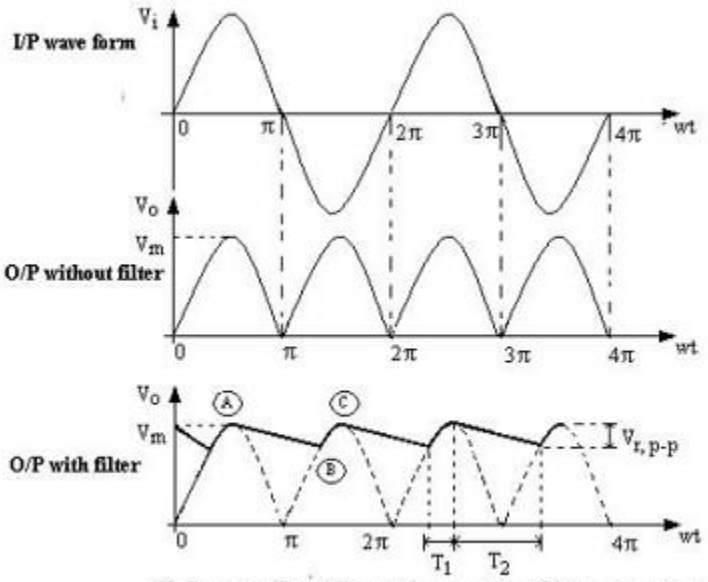


B) FULL WAVE RECTIFIER WITH FILTER:



MODEL WAVEFORMS:

WAVEFORMS:



Full-wave Rectifier with capacitor filter wave form

WITHOUT FILTER:

V no load Voltage (Vdc) = V

S.No	Load Resistance R_L kilo-ohms	O/P Voltage (Vo) V_{ac} (V)	O/P Voltage (Vo) V_{dc} (V)	Ripple factor $\left(\gamma = \frac{V_{ac}}{V_{dc}}\right)$	% of Regulation $\left(\frac{V_{NL} - V_{FL}}{V_{NL}} * 100\%\right)$
1	1				
2	2				
3	3				
4	4				
5	5				
6	6				
7	7				
8	8				

WITH CAPACITOR FILTER:

V no load Voltage (Vdc) = V

S.No	Load Resistance R_L kilo-ohms	O/P Voltage (Vo) V_{ac} (V)	O/P Voltage (Vo) V_{dc} (V)	Ripple factor $\left(\gamma = \frac{V_{ac}}{V_{dc}}\right)$	% of Regulation $\left(\frac{V_{NL} - V_{FL}}{V_{NL}} * 100\%\right)$
1	1				
2	2				
3	3				
4	4				
5	5				
6	6				
7	7				
8	8				

PROCEDURE:

1. Connections are made as per the circuit diagram.
2. Connect the ac mains to the primary side of the transformer and the secondary side to the rectifier.
3. Measure the ac voltage at the input side of the rectifier.
4. Measure both ac and dc voltages at the output side the rectifier.
5. Find the theoretical value of the dc voltage by using the formula Vdc = 2Vm/Π
6. Connect the filter capacitor across the load resistor and measure the values of Vac and Vdc at the output.
7. The theoretical values of Ripple factors with and without capacitor are calculated.
8. From the values of Vac and Vdc practical values of Ripple factors are calculated. The practical values are compared with theoretical values.

PRECAUTIONS:

1. The primary and secondary side of the transformer should be carefully identified.
2. The polarities of all the diodes should be carefully identified.

RESULT:

VIVA QUESTIONS:

1. Define regulation of the full wave rectifier?
2. Define peak inverse voltage (PIV)? And write its value for Full-wave rectifier?
3. If one of the diode is changed in its polarities what wave form would you get?
4. Does the process of rectification alter the frequency of the waveform?
5. What is ripple factor of the Full-wave rectifier?
6. What is the necessity of the transformer in the rectifier circuit?
7. What are the applications of a rectifier?
8. What is meant by ripple and define Ripple factor?
9. Explain how capacitor helps to improve the ripple factor?
10. Can a rectifier made in INDIA (V=230v, f=50Hz) be used in USA (V=110v, f=60Hz)?

EXPERIMENT NO. 3

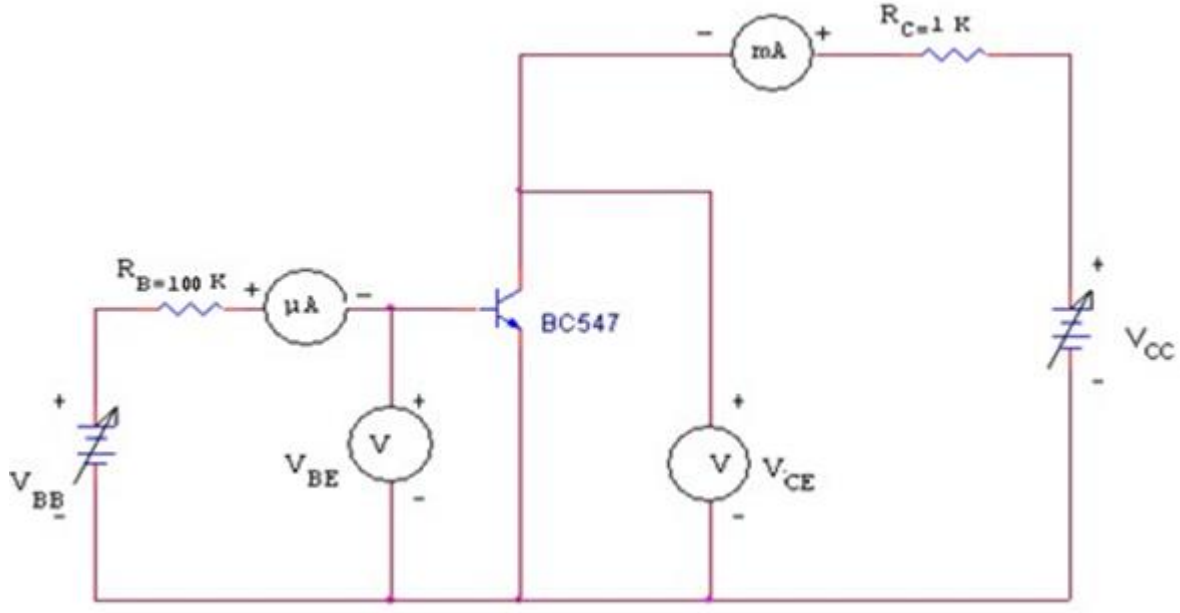
NPN BJT COMMON EMITTER CHARACTERISTICS

AIM: To study input and output characteristics of a NPN Bipolar Junction Transistor (BJT) in Common-emitter configuration.

COMPONENTS REQUIRED

Sl. No	APPARATURS AND COMPONENTS	Range	Quantity
01	BJT	BC-547B	1
02	Resistors	1KΩ, 100KΩ	1
03	VRPS	0-30V DC, 3A	1
04	CRO for testing		1
05	Signal generator	10Hz to 1MHz	1
06	Probes, wires		1
07	Ammeters	0- 10mA, 0- 100μ A	1

CIRCUIT DIAGRAM:



THEORY:

The transistor is a two junction, three terminal semiconductor device which has three regions namely the emitter region, the base region, and the collector region. There are two types of transistors. An npn transistor has an n type emitter, a p type base and an n type collector while a pnp transistor has a p type emitter, an n type base and a p type collector. The emitter is heavily doped, base region is thin and lightly doped and collector is moderately doped and is the largest. The current conduction in transistors takes place due to both charge carriers- that is electrons and holes and hence they are named Bipolar Junction Transistors (BJT).

BJTs are extensively used in all types of electronic circuits. The aim of this part of the experiment is to familiarize you with the basic modes of operation and features of a BJT. The BJT that you will be using in this experiment is BC 547 (the pin diagram is shown in Fig.1), which has a typical current rating of 100 mA (maximum).

Two of the most important applications for the transistor are (1) as an amplifier in analog electronic systems, and (2) as a switch in digital systems.

Basic Concepts The operation of the BJT is based on the principles of the pn junction. In the npn BJT, electrons are injected from the forward-biased emitter into the thin base region where, as minority carriers, they diffuse toward the reverse-biased collector. Some of these electrons recombine with holes in the base region, thus producing a small base current, IB. The remaining electrons reach the collector where they provide the main source of carriers for the collector current, IC. Thus, if there are no electrons injected from the emitter, there will be (almost) no collector current and, therefore, the emitter current controls the collector current. Combining currents, the total emitter current is given as IE = IB + IC. For normal pnp operation, the polarity of both voltage sources must be reversed.

Operation regions and characteristics curves:

Depending upon the biasing of the two junctions, emitter-base (EB) junction and collector- base(CB) the transistor is said to be in one of the four modes of operation. as described below:

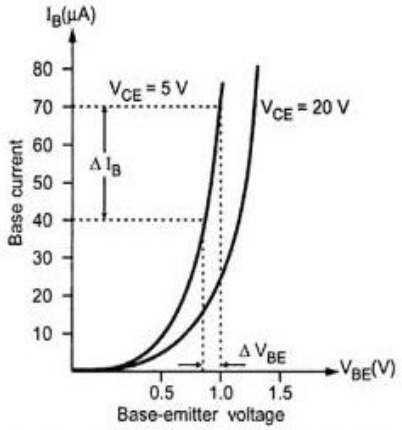
<table>
<tr><th>Operating region</th><th>B-E Junction</th><th>B-C Junction</th><th colspan="4">Features</th></tr>
<tr><td>Cut-off</td><td>Reverse</td><td>Reverse</td><td>IB ≈ IC≈IE≈0</td><td colspan="3">Off state – no current (VBE<0.7V)</td></tr>
<tr><td>Saturation</td><td>Forward</td><td>Forward</td><td>Conducting structure</td><td>VBE=0.7V</td><td colspan="2">VCE ≈ 0.2V</td></tr>
<tr><td>Active</td><td>Forward</td><td>Reverse</td><td>Amplifier Gain: 100-1000</td><td>(IC=βIB)</td><td>VBE=0.7V</td><td>VCE>0.2V</td></tr>
<tr><td>Reverse-active</td><td>Reverse</td><td>Forward</td><td>Limited use Gain< 1</td><td colspan="3">(IB>IC)</td></tr>
</table>

NOTE: VBE will vary from 0.6 to 0.7 V

The most important characteristics of transistor in any configuration are input and output characteristics.

Input Characteristics: -

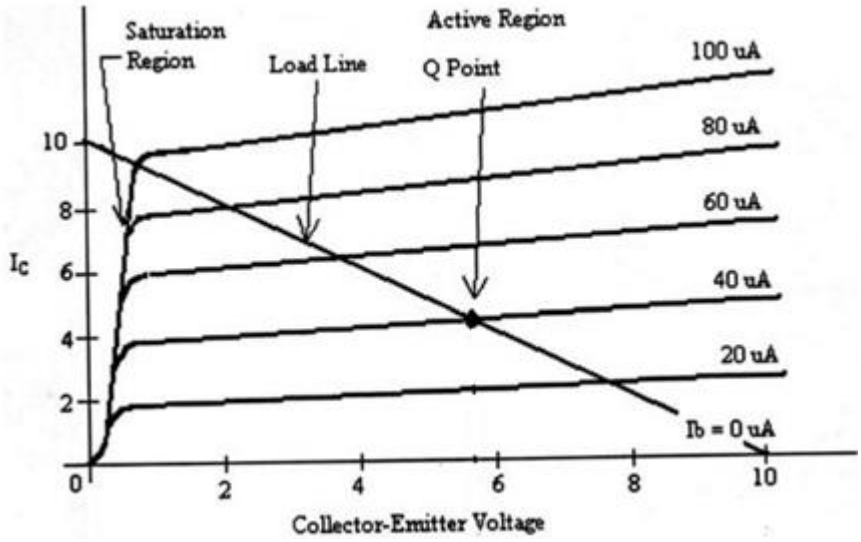
It is the curve between input current I_B and input voltage V_{BE} constant collector emitter voltage V_{CE}. The input characteristic resembles a forward biased diode curve. After cut in voltage the I_B increases rapidly with small increase in V_{BE}. It means that dynamic input resistance is small in CE configuration. It is the ratio of change in V_{BE} to the resulting change in base current at constant collector emitter voltage. It is given by $\Delta V_{BE} / \Delta I_B$



Input characteristics of the transistor in CE configuration

Output Characteristics:-

This characteristic shows relation between collector current I_C and collector voltage for various values of base current. The change in collector emitter voltage causes small change in the collector current for the constant base current, which defines the dynamic resistance and is given as $\Delta V_{CE} / \Delta I_C$ at constant I_B. The output characteristic of common emitter configuration consists of three regions: Active, Saturation and Cut-off.



Active region: In this region base-emitter junction is forward biased and base-collector junction is reversed biased. The curves are approximately horizontal in this region.

Saturation region: In this region both the junctions are forward biased.

Cut-off: In this region, both the junctions are reverse biased. When the base current is made equalto zero, the collector current is reverse leakage current I_{CEO}. The region below $I_B = 0$ is the called the cut-off region.

OBSERVATION:

INPUT CHARACTERISTICS:

VBB	VCE=2V		VCE=3V(Choose value which utook in lab)	
	VBE (V)	IB (µA)	VBE (V)	IB (µA)
0.1				
0.2				
.				
1				
1.5				
.				
5				

OUTPUT CHARACTERISTICS

VCC	IB =10(µA)		IB =20(µA)(Choose value whichu took in lab)	
	VCE (V)	Ic (mA)	VCE (V)	Ic(mA)
0				
0.2				
.				
.				
1				
1.5				
.				
.				
5				
6				
.				
20				

PROCEDURE:

A. Input Characteristics:

1) Make the circuit connection as shown in the circuit diagram.
2) Set the voltage VCE = 2 V and vary IB with the help of VBB and measure VBE.
3) Set the voltage VCE = 3 V and vary IB with the help of VBB and measure VBE.
4) Plot graph of IB v/s VBE.
5) Evaluate dynamic input resistance which is the ratio of change in VBE to the resulting change in base current at constant collector emitter voltage. It is given by ΔVBE / ΔIB
6) The reciprocal of the slope of the linear part of the characteristic gives the dynamic input resistance of the transistor.

B. Output Characteristics:

1) Keep IB constant say 10 μA, vary VCE and note down the collector current IC.
2) Now keep IB = 20 μA, vary VCE and note down the collector current IC.
3) Plot graph of IB v/s VCE.
4) The change in collector emitter voltage causes small change in the collector current for the constant base current, which defines the dynamic output resistance and is given as ΔVCE / ΔIC at constant IB or the output conductance is given ΔIC/ΔVCE with the IB at a constant current.
5) Find output conductance from the slope of the linear portion of the characteristic curves and also find small-signal current gain which is calculated by β = ΔIC/ΔIB with the VCE at a constant voltage.

CALCULATION:

1. Small-Signal Current Gain: β = ΔIC/ΔIB with the VCE at a constant voltage.
2. Dynamic input resistance: It is given by ΔVBE / ΔIB at constant VCE
3. Dynamic output resistance: It is given as ΔVCE / ΔIC at constant IB

RESULTS:

1. Small-Signal Current Gain: _____
2. Dynamic input resistance: _____
3. Dynamic output resistance: _____

Add Graphs for the input and output characteristics:

CONCLUSION:

VIVA QUESTIONS:

1. What is the function of base region of a transistor? Why this region is made thin and lightly doped?
2. What is the voltage across the collector to emitter terminal when the transistor is in
   (i) saturation (ii) cut-off (iii) active region?
3. Describe, based on your observations, the I-V curves of npn transistor. At approximately what collector-emitter voltage (VCE) does the transition from saturation to active region occur?
4. Describe the necessary conditions operation in the active region in terms of VBE and VCE.
5. Explain early effect?

EXPERIMENT NO. 3

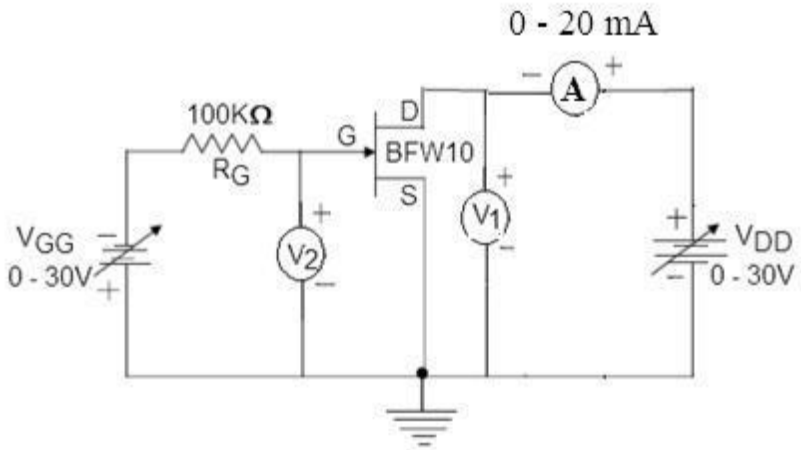
JFET CHARACTERISTICS

AIM: Plot the transfer and drain characteristics of a JFET and calculate its drain resistance, mutual conductance and amplification factor.

COMPONENTS REQUIRED

Sl. No	APPARATURS AND COMPONENTS	Range	Quantity
01	JFET	BFW10	1
02	Resistor	100KΩ	1
03	VRPS	0-30V DC, 3A	1
04	CRO for testing		1
05	Signal generator	10Hz to 1MHz	1
06	Probes, wires		1
07	Ammeters	0- 10mA, 0- 100μ A	1

CIRCUIT DIAGRAM:



Procedure:

Set up the connections as indicated in the figure. V1 and V2 are Voltmeters (or multimeter) and A is ammeter (multimeter)

Follow the below procedure to obtain the drain characteristics:

1. Adjust the reading of V2 to
   a. +0.5V by interchange the polarity VGG
   b. 0V (Short the gate terminal to ground)
   c. –1V, –2V and – 3V.

2. For every constant VGG values (+0.5, 0, -1, -2, -3 etc) vary VDD voltage such that V1 is as indicated in the table below and record the corresponding readings of ID.

VGS = V2 = Constant (0.5V, 0V, - 1V, - 2V, - 3V)

$V_1(V_{DS}, V)$	0.1	0.15	0.2	0.25	0.3	0.4	0.6	0.8	1.0	1.2	1.4	1.6	1.8
I_D, mA													
$V_1(V_{DS}, V)$	2	2.4	2.8	3.0	3.4	3.6	3.8	4.0	5.0	6	8	10	12
I_D, mA													

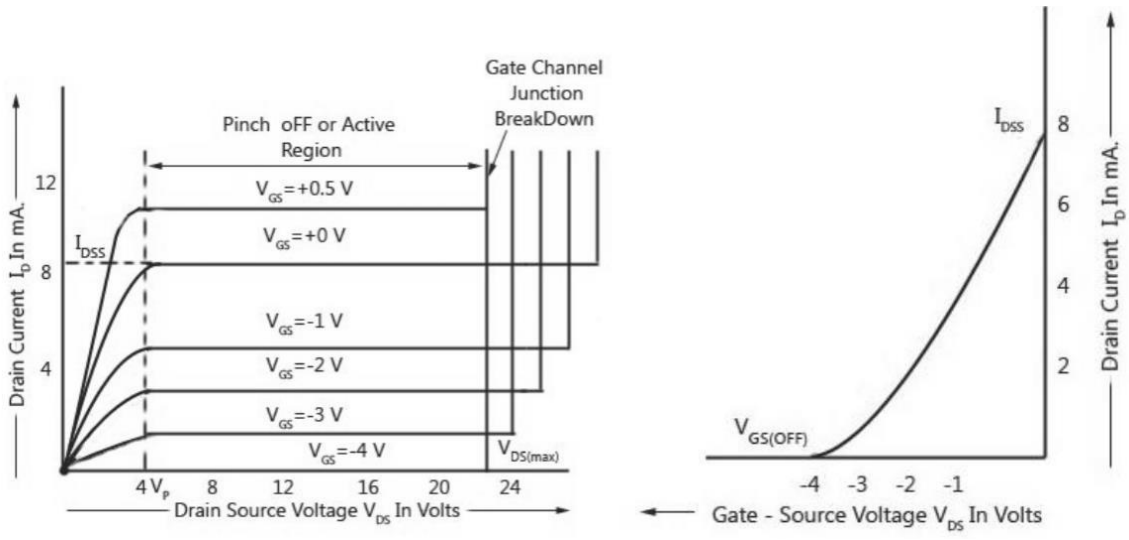
Follow the below mentioned procedure to obtain transfer characteristics:

1. Set VDS = 6V. This can be done by adjusting the reading of V1 to 6V.
2. Record the readings of ID for different values of V2 as indicated in the table.
3. Repeat step one and 2 for VDS = 9V and VDS = 12V

$V_2(V_{GS}, V)$	0	−0.2	−0.4	−0.6	−0.8	−1.0	−1.2	−1.4	−1.6	−1.8	−2.0
I_D, mA											
$V_2(V_{GS}, V)$	−2.2	−2.4	−2.6	−2.8	−3.0	−3.2	−3.4	−3.6	−3.8	−4.0	
I_D, mA											

NOTE: *For the drain characteristics, take at least 3 readings before and after the pinch-off starts (assumed pinch off voltage 4V) so that you will get a smooth graph. For the transfer characteristics keep increasing |V2| till drain current becomes zero.*

EXPECTED GRAPHS:



a) Drain Characteristics

b) Transfer Characteristics

Observations:

1. From the graphs determine
2. $g_m = (\Delta I_D/\Delta V_{GS})|_{VDS = Constant}$
3. $rd = (\Delta I_D/\Delta V_{DS})|_{VGS = Constant}$

Add Graphs for the input and output characteristics:

CONCLUSION:

VIVA QUESTIONS:

1. Explain the differences between a BJT and a JFET and compare them?
2. Briefly explain about unipolar device. Is JFET a unipolar device, Justify your answer?
3. Give the symbols of JFET and MOSFET?
4. List the major applications of a JFET?
5. Briefly explain the characteristic parameters of a FET and give the relations between them?
6. Mention the differences between n-channel and p-channel JFETs?
7. List the types of JFET configurations. Give the applications of each configuration?
8. Explain about MOSFET and the possible types in a MOSFET?
9. Give the drain current and Trans conductance equation in JFET?

EXPERIMENT NO. 5

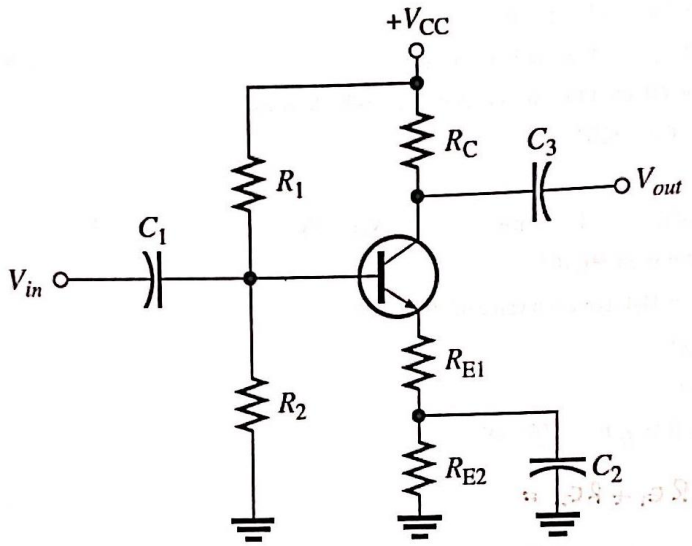
FREQUENCY RESPONSE OF SINGLE STAGE RC – COUPLED AMPLIFIER

AIM: To determine the frequency response of single stage RC – Coupled Amplifier.

COMPONENTS REQUIRED

Sl. No	APPARATURS AND COMPONENTS	Range	Quantity
01	BJT	BC-547B	1
02	Resistors	3.3KΩ, 33KΩ, 330Ω	2
03	VRPS	0-30V DC, 3A	1
04	CRO for testing		1
05	Signal generator	10Hz to 1MHz	1
06	Probes, wires		1
07	Capacitors	20μF, 47μF	2

CIRCUIT DIAGRAM:



Procedure:

1. Set up the circuit as shown in the Fig. and set V_{CC} to 10V.
2. Ensure that V_{CE} is around 5V. Adjust R_2 if necessary.
3. Calculate the voltage gain with sinusoidal input of 100 mV(p-p) at 1KHz. Input amplitude can be set to any convenient value so that output is undistorted.
4. Obtain the frequency response by varying the input frequency from 10Hz-1MHz in suitable steps and record the output voltage in Table 2.1.
5. Measure the input and output impedance at 1KHz.
6. Plot the graphs for $|A_v|_{dB}$ versus frequency on the semi log sheet.
7. Calculate the mid band gain, lower and upper cut-off frequencies and bandwidth.
8. Tabulate the results in Table 2.2
9. Compare the practical values of voltage gain and input impedance with theoretical values.
10. Observe the effect of R_{E1} on the gain and input impedance, by varying R_{E1}.

Measurement of Z_i:

1. Set the frequency at 1 KHz and ensure that the output signal is undistorted. Note down the output voltage.
2. Now connect a potentiometer between A and B, with pot kept at its minimum position. The pot value should be little higher than $Z_{i(\text{ theoretical})}$.
3. Slowly increase the pot resistance until the output reduces to half of its previous value.
4. Remove the pot and measure its resistance. It gives the input impedance

Measurement of Z_o:

1. Set the frequency at 1KHz and ensure that the output signal is undistorted. Note down the output voltage.
2. Connect a pot whose value is little higher than $Z_{o(\text{ theoretical})}$, between the output terminals. Initially the pot must be kept at its maximum value.
3. Slowly decrease the pot resistance until the output reduces to half of its previous value.
4. Remove the pot and measure the resistance. It gives the output impedance.

Effect of Loading:

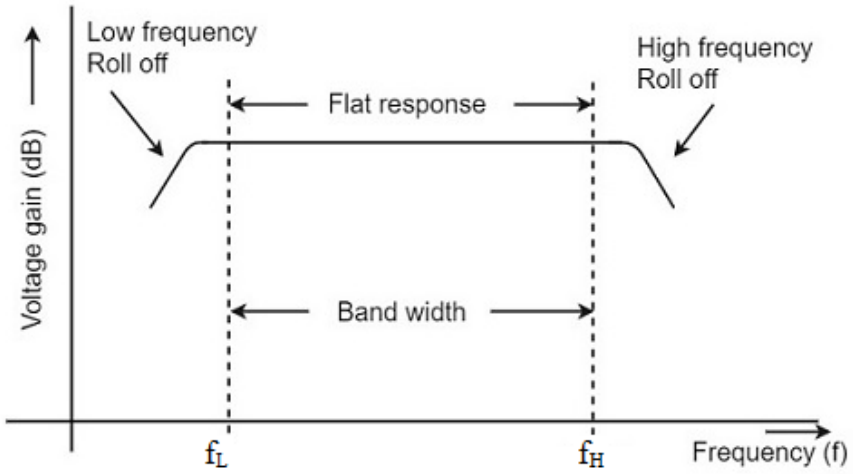
1. Connect R_L=22KΩ, 10KΩ, 4.7KΩ, 2.2KΩ, and 1KΩ, and for each value of R_L, calculate the gain and record in Table 2.3.
2. R_L should be connected between C and D and the frequency should be set at 1 KHz.
3. Compare the theoretical and practical gains.
4. Comment on the effect of R_L on gain.

Table 2.1: Frequency Response of single stage RC coupled CE amplifier

Frequency	$V_{i(p-p)}$	$V_{o(p-p)}$	A_V	$\|A_V\|_{dB}$

Frequency Response of RC Coupled Amplifier

Frequency response curve is a graph that indicates the relationship between voltage gain and function of frequency. The frequency response of a RC coupled amplifier is as shown in the following graph.



Inference:

Table 2.2: Comparison of practical and theoretical values

	Theoretical values with equations	Practical values
Mid band voltage gain		
Input impedance		
Output impedance		
Cut-off frequencies		Lower cut-off frequency: Upper cut-off frequency:
Bandwidth		
MSHC		

Inference:

Add Graphs for the input and output characteristics:

VIVA QUESTIONS:

1. What is an RC Coupled Amplifier?
2. What are the Applications of RC Coupled Amplifier?
3. What do you mean by Decibel?
4. What do you mean by frequency response?
5. What are the requirements of an ideal coupling network?
6. What do you mean by the bandwidth of an amplifier?

EXPERIMENT NO. 6

RC– Low pass and High Pass filters.

Aim: To design RC low pass and high pass filter circuits and

a. Obtain the frequency response
b. Find the cut off frequencies and phase differences between output and input voltages.
c. Study square wave response

A) Design of Low pass filter:

Specifications:

- Cut off frequency, f_c= 500 Hz.
- $f_c = \frac{1}{2\pi RC}$
- Select C<1μF and find R.

  R =

Circuit Diagram:

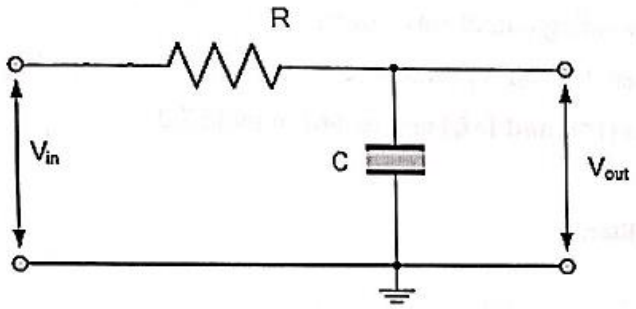


Figure 1: Circuit diagram of low pass filter

Figure 2: Frequency response

Theoretical equations for $|A_v|$ and Θ With sine wave input:

$|A_v|$ =

Θ =

Expected output waveform with sine wave input:

Expected output waveforms with square wave input at frequencies $f < f_c$ and $f > f_c$:

Procedure:

1. Set up the circuit as shown in the Figure .1.
2. Apply sine wave input of 100 $mV_{(P-P)}$ or any suitable amplitude of frequency 1KHz and measure $V_{0(P-P)}$.
3. Obtain frequency response and tabulate the results in table 7.1.Plo tthe frequency response, calculatethe cut off frequency and compare it with the theoretical value.
4. Observe the output for square wave input for at least five frequencies ($f < f_c$ **and** $f > f_c$) and plot the corresponding output waveforms.
5. Measure the phase difference between V_o and V_i with sine wave input of constant amplitude at five different frequencies ($f<f_c$ **and** $f>f_c$) and record in table .2.

Table .1: Frequency Response of Low Pass Filter.

$V_{i(p-p)}$ =

Frequency	$V_{o(p-p)}$	$A_V = \frac{V_o}{V_i}$	$\lvert A_V \rvert_{dB} = 20 \log_{10}\left(\frac{V_o}{V_i}\right)$	$\lvert A_V \rvert_{dB}$ (Theoretical)

Inference:

Table 2: Phase Difference between Input and Output Voltages.

Frequency	H-intercept	Y-intercept	$\Theta = sin^{-1}\left(\frac{y}{H}\right)$(Practical)	Θ (Theoretical)

Inference:

Output Waveforms with Square wave input at FIVE different frequencies:

($f = f_c/5$, $f_c/2$, f_c , $2f_c$ & $5f_c$)

Expected output waveforms with square wave input at frequencies $f < f_c$ and $f > f_c$:

Procedure:

1. Set up the circuit as shown in the Figure 3.
2. Apply sine wave input of 100 $mV_{(P-P)}$ or any suitable amplitude of frequency 1KHz and measure $V_{0(P-P)}$.
3. Obtain frequency response and tabulate the results in table 3.Plot the frequency response, calculate the cut off frequency and compare it with the theoretical value.
4. Observe the output for square wave input for at least five frequencies ($f < f_c$ **and** $f > f_c$) and plot the corresponding output waveforms.
5. Measure the phase difference between V_o and V_i with sine wave input of constant amplitude at five different frequencies ($f<f_c$ **and** $f>f_c$) and record in table 4.

Table 3: Frequency Response of High Pass Filter.

$V_{i(p-p)}$ =

Frequency	$V_{o(p-p)}$	$A_V = \frac{V_o}{V_i}$	$\lvert A_V \rvert_{dB} = 20 \log_{10}\left(\frac{V_o}{V_i}\right)$	$\lvert A_V \rvert_{dB}$ (Theoretical)

Inference:

Table 4: Phase Difference between Input and Output Voltages.

Frequency	H-intercept	Y-intercept	$\Theta = sin^{-1}\left(\frac{y}{H}\right)$(Practical)	Θ (Theoretical)

Inference:

Output Waveforms with Square wave input at FIVE different frequencies:

($f = f_c/5$, $f_c/2$, f_c , $2f_c$ & $5f_c$)

Inference:

Add Graphs for the input and output characteristics:

VIVA QUESTIONS:

1. A device that separates disturbances from a signal is ____?
2. What are the applications of filter?
3. Define High Pass and low pass filter
4. Why are active filters preferred
5. Difference between active and passive filters.

EXPERIMENT NO. 7

BJT-DARLINGTON EMITTER FOLLOWER CIRCUIT

AIM:

To design and test a Darlington emitter follower circuit with and without boot strapping and determine the gain, input and output impedance.

COMPONENTS REQUIRED:

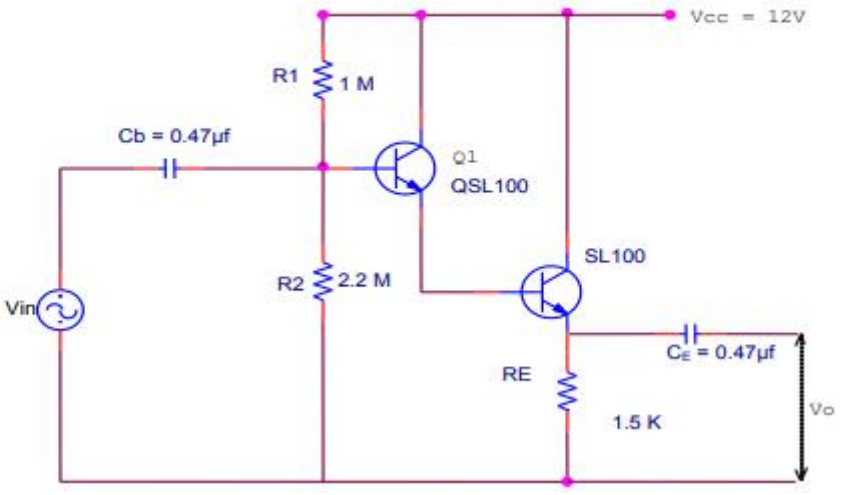
Sl. No.	Components Details	Specification	Qty
1.	Transistor	SL100	2 Nos.
2.	Capacitors	10 μf	1 No
		0.47μf	2 Nos.
3.	Resistors	1 MΩ, 2.2 MΩ, 1.5 KΩ, 10 KΩ, 47KΩ	Each 1 No
	DC Supply, CRO with Probe, Signal generator, AC millivoltmeter		

THEORY:

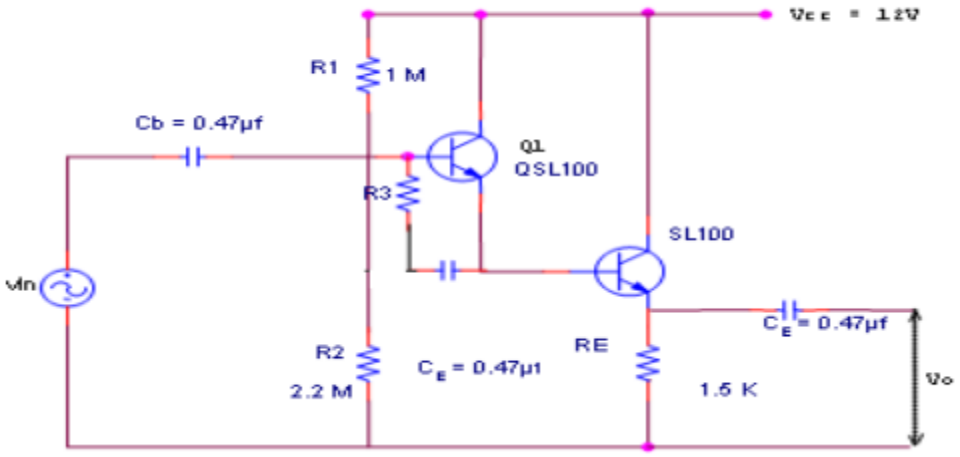
Normally transistors are used as amplifiers. But there are some applications in which, matching of impedance is required between two circuits without any gain or attenuation. In such applications emitter followers are used. Emitter followers have large input impedance and small output impedance. Darlington emitter follower has two transistors connected in cascade such that the emitter of first transistor is connected to the base of second transistor. The voltage gain of the darlington emitter follower is close to unity. The major drawback of this circuit is that the second transistor amplifies leakage current of the first transistor and overall leakage current becomes high. The output is observed at the emitter terminal of the second transistor. Hence it is called an emitter follower.

CIRCUIT DIAGRAM:

Darlington emitter follower without bootstrapping



Darlington emitter follower with bootstrapping



DESIGN:

Given I_C = 4mA, V_{CC} = 12V, V_{BE} = 0.6V, $\beta_1 = \beta_2$ = 100

To find R_E:

Applying KVL to the output loop of the second transistor, we get

$V_{CC} = V_{CE} + V_{RE}$

Therefore $V_{RE} = V_{CC} - V_{CE} = 12 - 6$

Therefore V_{RE} = 6V

W.K.T $R_E = V_{RE} / I_{E2}$

Here $I_{E2} = I_{C2}$

Therefore $R_E = 6 / 4 \times 10^{-3}$

R_E = 1.5kΩ

To find R_1 & R_2:

From the circuit we have

$V_A = V_{BE1} + V_{BE2} + V_{RE}$

$= 0.6 + 0.6 + 6 = 7.2V$

W.K.T. $I_C = \beta IB$

Therefore $I_B = (4 \times 10^{-3}) / 100 = 40\ \mu A$

Let $10I_B$ be the current through R_1 and $9I_B$ be the current through R_2.

From the fig. we see that

$R_1 = (V_{CC} - V_A) / 10I_B$

Therefore **R_1 = 12KΩ**

From the fig. $R_2 = V_A / 9I_B$

Therefore **R_2 = 20 KΩ ≈ 22KΩ**

W.K.T. $C_C = 10 / X_{RE} = 10 / (2.\pi.f.R_E)$

Assume f = 50Hz

Therefore $\mathbf{C_C = 21.2\mu F \approx 47\ \mu F}$

W.K.T. $C_b = 10 / X_{RB} = 10 / (2.\pi.f.R_B)$ where $R_B = R_1 \,||\, R_2 = 7.5k\Omega$

Therefore $\mathbf{C_b = 4.2\mu F \approx 4.7\mu F}$

Chose $\mathbf{R_3 = 10\ K\Omega}$, $\mathbf{C_B = 10\mu f}$ for bootstrapping

PROCEDURE:

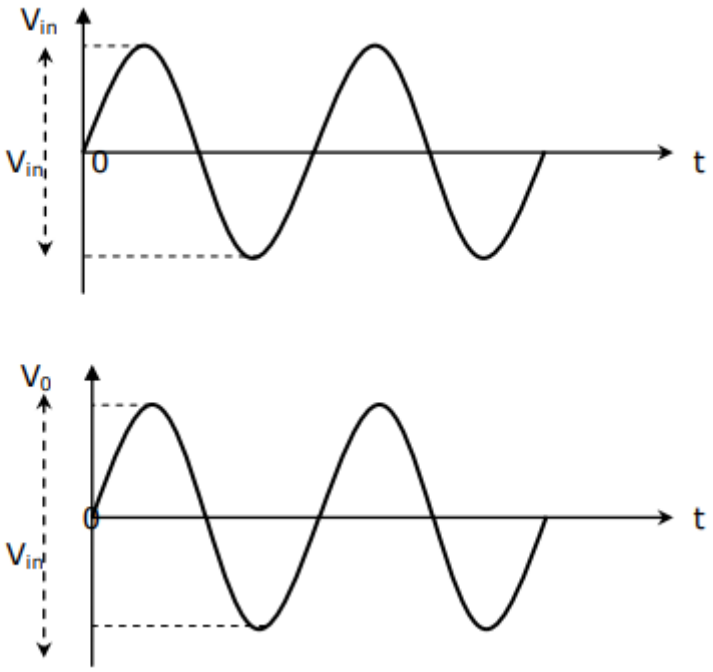
1. Rig up the circuit as shown in the fig.
2. Check the circuit for biasing, i.e. check V_{CE}, V_{CC} and V_{RE}.
3. Give a sinusoidal input signal of 1KHz from a signal generator.
4. Set the input signal to a value such that the output doesn't get clipped.
5. For different frequencies of the input signal, read the output on the voltmeter and verify that the gain is 1.
6. To measure input impedance, connect a resistor of 47kΩ in series with the signal generator.
7. Measure the voltage at the input point (V_S) and at the point after the resistor (V_{IN}).
8. Current through the resistor is given by the expression $\mathbf{I = (V_S - V_{IN}) / 47K}$.
9. Input impedance is given by $\mathbf{Z_{IN} = V_{IN} / 47\ K}$
10. To measure output impedance, connect a DRB in parallel with the output.
11. Adjust all the knobs of the DRB to maximum.
12. Start reducing the resistance in the DRB from a large value until the output reduces to half.
13. The resistance in the DRB is the output impedance.

TABULAR COLUMN:

V_{IN} = _____ constant

Frequency (Hz)	V_0 (V)	A_V	A_V (dB)

WAVEFORM:



Result:

VIVA QUESTIONS:

1. Why do you need more than one stage of amplifiers in practical circuits?
2. What is the effect of cascading on gain and bandwidth?
3. What happens to the 3dB frequencies if the number of stages of amplifiers increases?
4. Why we use a logarithmic scale to denote voltage or power gains, instead of using the simpler linear scale?
5. What is loading effect in multistage amplifiers?

EXPERIMENT NO. 8

VOLTAGE SERIES FEEDBACK AMPLIFIER

Aim: To design and test the Voltage-series feedback amplifier and to calculate the following parameters with and without feedback.

1. Mid band gain.
2. Bandwidth and cut-off frequencies.
3. Input and output impedance

FACILITIES REQUIRED AND PROCEDURE

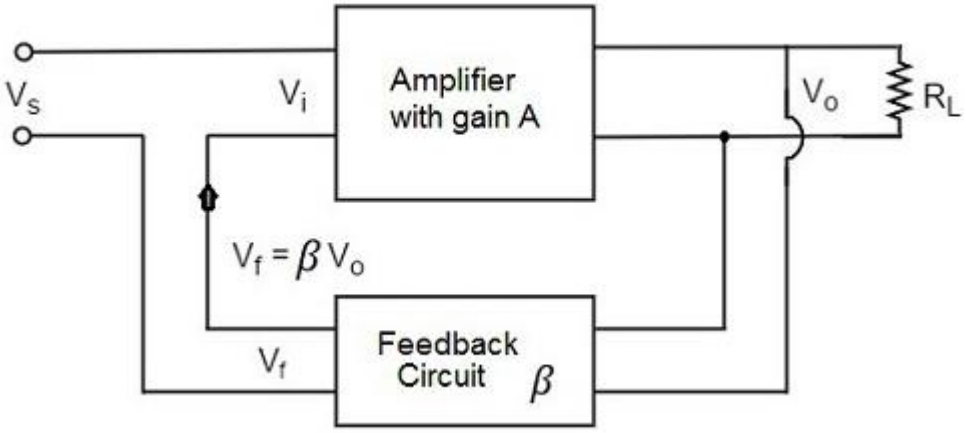
FACILITIES REQUIRED TO DO THE EXPERIMENT:

S.NO	APPARATUS	SPECIFICATION	QUANTITY
1.	Power supply	(0-30)V	1
2.	Function Generator	(0-20M)Hz	1
3.	CRO		1
4.	Transistor	BC107	1
5.	Resistor		
6.	Capacitor		
7.	Connecting Wires		

THEORY:

Voltage-Series Feedback: In the voltage series feedback circuit, a fraction of the output voltage is applied in series with the input voltage through the feedback circuit. This is also known as shunt-driven series-fed feedback, i.e., a parallel-series circuit.

The following figure shows the block diagram of voltage series feedback, by which it is evident that the feedback circuit is placed in shunt with the output but in series with the input.



PROCEDURE:

1. Connect the circuit as per the circuit diagram.
2. Keeping the input voltage constant, vary the frequency from 50Hz to 3MHz in regular steps and note down the corresponding output voltage.
3. Plot the graph: Gain (dB) Vs Frequency
4. Calculate the bandwidth from the graph.
5. Calculate the input and output impedance.
6. Remove Emitter Capacitance, and follow the same procedures (1 to 5).

DESIGN PROCEDURE/ DESIGN CALCULATIONS:

(i) Series Feedback Amplifier: Without Feedback:

$V_{CC} = 12V;\quad I_C = 1mA;\quad f_L = 50Hz;\quad S = 2;\ R_L = 4.7K\Omega$

$r_e = \frac{26mV}{I_c} =$

$V_{ce} = \frac{V_{cc}}{2} =$

$V_E = {}^{V_{cc}}/_{10}\ h_{ie} = h_{fe} r_e;$

Applying KVL output loop, we get $V_{cc} = I_E R_E + I_C R_C + V_{ce};$

$R_C =$

$R_L = 4.7K\Omega$

Since I_B is very small when compare with $I_C, I_C \approx I_E$

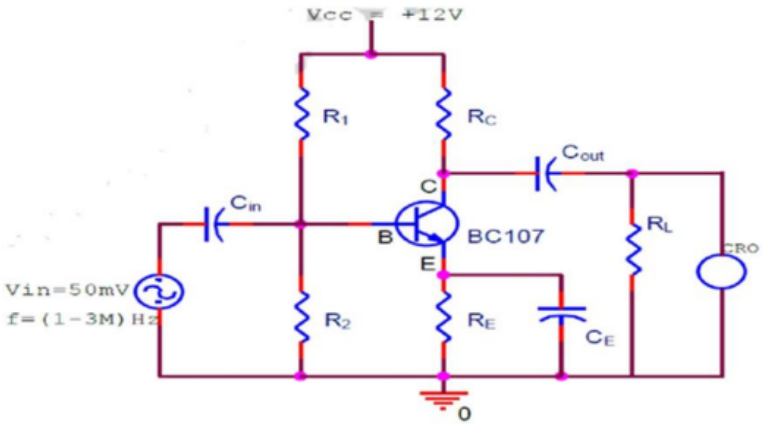
$R_E = \frac{V_E}{I_E};\qquad S = 1 + \frac{R_B}{R_E}$

$R_B =$

$V_B = \frac{V_{CC} R_2}{(R_1 + R_2)}\quad R_B = R_1 // R_2$

$R_1 = \qquad R_2 =$

$X_{Ci} = \frac{h_{ie} // R_B}{10}\quad C_i = \frac{1}{2\pi f X_{ci}}\quad X_{Co} = \frac{R_C // R_L}{10}\quad C_o = \frac{1}{2\pi f X_{co}}$



With feedback (Remove the Emitter Capacitor, C_E):

Feedback factor, $\beta = -R_E =$

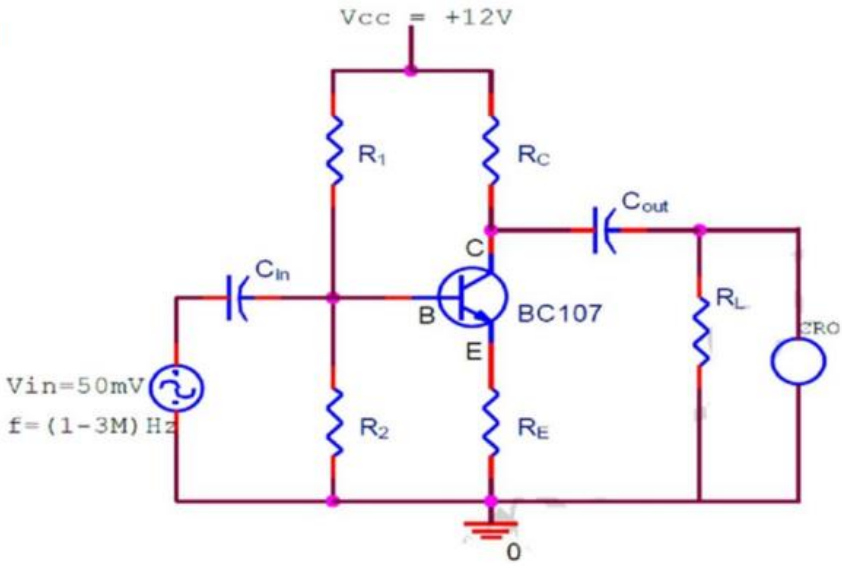
$G_m = -h_{fe} / (h_{ie} + R_E) =$

Desensitivity factor, $D = 1 + \beta G_m =$

Transconductance with feedback, $G_{mf} = G_m / D =$

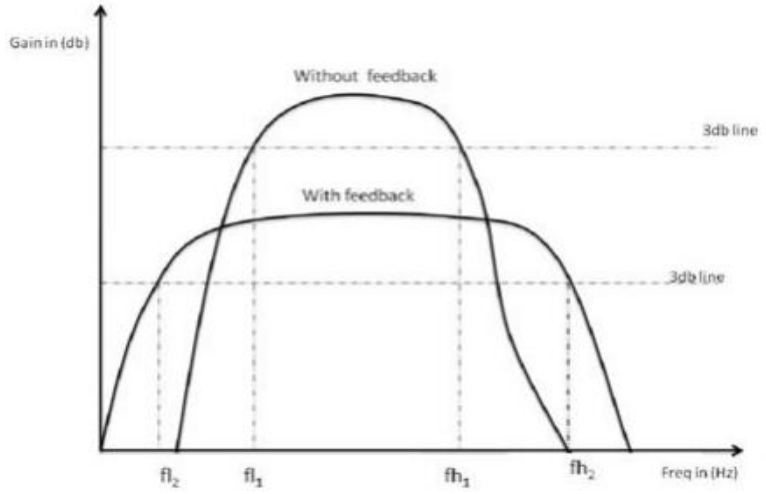
Input impedance with feedback, $Z_{if} = Z_i D$

Output impedance with feedback, $Z_{0f} = Z_0 D$



MODEL GRAPH:

Series Feedback Amplifier



TABULATION:

(i) Without Feedback:

Frequency (Hz)	Vo (Volts)	Gain = Vo/Vi	Gain = 20 log(Vo/Vi) (dB)

(ii) With Feedback:

Frequency (Hz)	Vo (Volts)	Gain = Vo/Vi	Gain = 20 log(Vo/Vi) (dB)

Inference:

VIVA QUESTIONS:

1. What is the difference between positive feedback and negative feedback?
2. Define Sensitivity?
3. What are the applications of feedback amplifiers?
4. What is the effect of current series feedback amplifier on the input impedance of the amplifier?
5. Mention the properties of negative feedback?
6. Give an example of negative shunt feedback?
7. Define voltage shunt feedback?
8. What is the effect of negative feedback on the bandwidth of an amplifier?

EXPERIMENT NO. 9

NEGATIVE FEEDBACK AMPLIFIER

AIM:

To study the effect of negative feedback amplifier on:

i) Gain.

ii) Bandwidth.

iii) Input and Output Impedances.

Design Specifications:

- $A_v = -50$, $V_{CC} = 10V$
- $V_{CE} = 5V$, $I_C = 2mA$
- Transistor used: BC107
- $\beta_{dc} = h_{FE} = 180$ (Typical value)

Design Procedure:

- $A_V = -\frac{R_C}{r_e}$ ..... (1)

Find R_C using equation (1)

$r_e =$

$R_C =$

- $V_{CC} = I_C R_C + V_{CE} + I_E R_E$ ..... (2)

Find R_E using equation (2)

$R_E =$

- $R_2 \leq \frac{\beta R_E}{10}$ ..... (3)

Find R_2 using equation (3)

$R_2 =$

- $V_{TH} = V_{BE} + V_E$

$V_E = I_E R_E$

$V_{TH} =$

- $V_{TH} = \frac{V_{CC} R_2}{R_1 + R_2}$ ..... (4)

Find R_1 using equation (4)

$R_1 =$

- Select $C_1 = C_2 = 10\mu F$ and $C_E = 47\ \mu F$

Circuit Diagram:

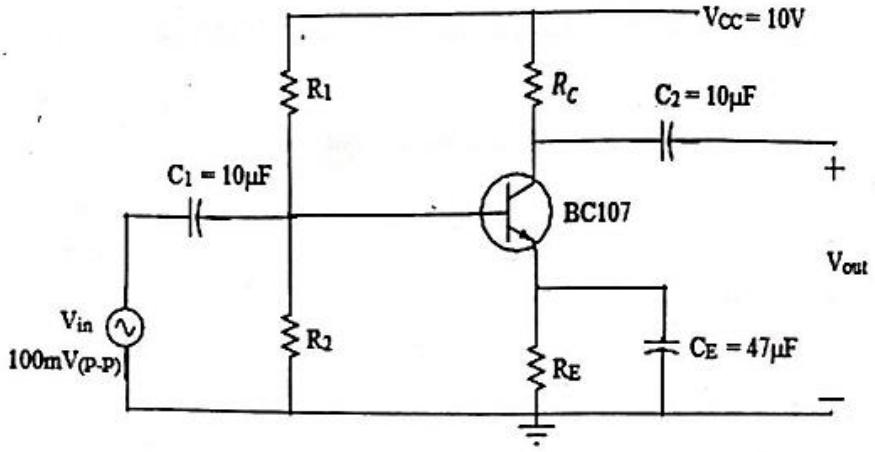


Fig. 1: Circuit Diagram of negative feedback amplifier

Theoretical Values of Z_{in} and Z_o with relevant equations:

1) Z_{in}(without C_E)

2) Z_{in}(with C_E)

3) Z_o(without C_E)

4) Z_o (without C_E)

Procedure:

1. Connect the circuit as shown in Fig.8.1.
2. Obtain frequency response and tabulate the results in table 1 and measure bandwidth and mid band gain.
3. Measure Z_{in} and Z_o.
4. Now remove $C_E$repeat steps (2) and (3). Tabulate the results in table 2.
5. Compare the results obtained in (2)&(3) with that of (4) and evaluate the effect of negative feedback on gain, bandwidth,$Z_{in}$and $Z_o$with proper reasoning and tabulate the results in table 3.
6. Verify that with negative feedback the circuit works as an ideal voltage to current converter. i.e.,$I_{C\ (ac)} \alpha V_{in}$and tabulate the readings in table 4.

Table 1: Frequency Response of negative feedback amplifier with C_E(Without Feedback)

Frequency	$V_{i(p-p)}$	$V_{o(p-p)}$	$A_V = \frac{V_o}{V_i}$	$\lvert A_V \rvert_{dB} = 20 \log_{10}\left(\frac{V_o}{V_i}\right)$

Table 2: Frequency Response of negative feedback amplifier withoutC_E(With Feedback)

Frequency	$V_{i(p-p)}$	$V_{o(p-p)}$	$A_V = \frac{V_o}{V_i}$	$\lvert A_V \rvert_{dB} = 20 \log_{10}\left(\frac{V_o}{V_i}\right)$

Table 3: Comparison Table

	Theoretical values		Practical values	
	Without Feedback	With Feedback	Without Feedback	With Feedback
Midband voltage gain				
Input impedance				
Output impedance				
Bandwidth				

Table 4: Voltage to Current Conversion

V_{in}	$I_{C\,(ac)}$

Inference with result interpretation:

VIVA QUESTIONS:

1. What is negative feedback in an amplifier?
2. Why negative feedback is preferably used in op-amp?
3. Why is negative feedback important?
4. Applications of negative feedback

EXPERIMENT NO. 10

OSCILLATORS: HARTLEY OSCILLATOR / COLPITT'S OSCILLATOR

AIM: Design and set-up the following tuned oscillator circuits using BJT, and determine the frequency of oscillation.

COMPONENTS REQUIRED:

Sl. No.	Components Details	Specification	Qty
1.	Transistor	SL100	1 No
2.	Capacitors	0.1 μ*f*, 1000 *pf*	2 No
		47μ*f*, 0.0023 μ*f*	Each 1 No
3.	Resistors	22KΩ, 4.7KΩ, 1.2KΩ, 330Ω 1 K Pot	Each 1 No
4.	Inductors	100 μH, 1mH, 5mH	Each 1 No
	DC Supply, CRO with Probe		

THEORY:

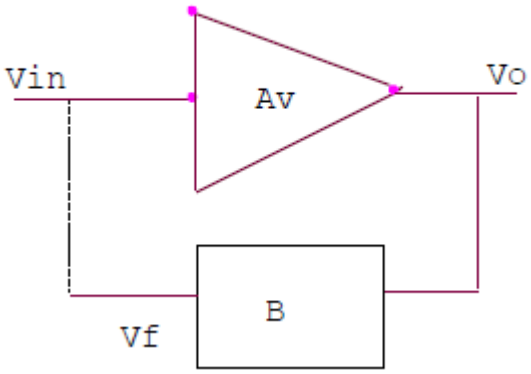
Oscillators are devices, which generate oscillations. The frequency of oscillations depends on the feedback network. Feedback may be of two types namely positive and negative. In positive feedback, the feedback signal is applied in phase with the input signal thus increasing it. In negative feedback, the feedback signal is applied out of phase with the input thus reducing it. The feedback used in oscillators is positive feedback. The oscillators work on the principle of Barkhausen criteria. This states that for sustained oscillations

i) Loop gain Avβ must be equal to 1.

ii) The phase shift around the loop must be 0 deg of 360 deg.

Here Av is the gain of the amplifier and β is the attenuation of the feedback network. Consider the feedback network shown in the fig (1) below. Assume an amplifier with input signal Vin. The output signal VO will be 180 deg out of phase with Vin. So to get an in phase output, the feedback network provides 180-deg phase shift. Therefore the output Vf from the feedback network can be made in phase and equal in amplitude to Vin and Vin can be removed. Even then the oscillations continue. Practical oscillations do not need any input signal to start oscillations. They are self-starting due to thermally produced noise in resistors and other components. Only one frequency (fo) of noise satisfies, Barkhausen criteria and the circuit oscillates with that frequency. The magnitude of fo keeps on increasing each time it goes around the loop. The amplification of fo is limited by circuit‟s own non-linearities. Therefore to start oscillations Avβ > 1 and to sustain it, the loop gain Avβ = 1.

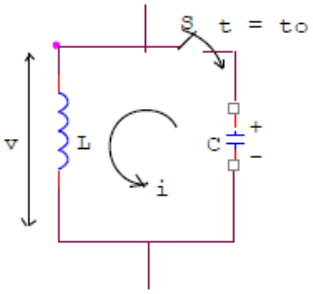
Fig 1. Amplifier



The feedback network used here consists of L and C. Consider the circuit shown below fig 2. This circuit consists of L and C in parallel. The capacitor stores energy in its electric field whenever there is voltage across it and the inductor stores energy in its magnetic field whenever there is current through it. Initially let us assume that the capacitor has charged to V volts. When S is closed c= 0. When S is closed at t = t0 , capacitor starts charging through the inductor. Thus a voltage gets built up across the inductor due to the change in current through it. If the capacitor was changed with the polarity as shown in the fig 2 the current starts flowing from the positive plate of the capacitor to the negativ4 plate of the capacitor. As shown the voltage across the capacitor reduces during the discharge time v reduces and I increases. At time t1 v will be 0 and I will be maximum as c is fully discharged, the capacitor charges like sinusoidal oscillations. Thus the circuit oscillates with the frequency

$fo = 1/ 2\pi\sqrt{LC}$

Fig.2



The Hartley oscillator consists of two inductors and a capacitor and Colpitts oscillator consists of two capacitors and an inductor.

The resonant frequency fo for Hartley oscillator is

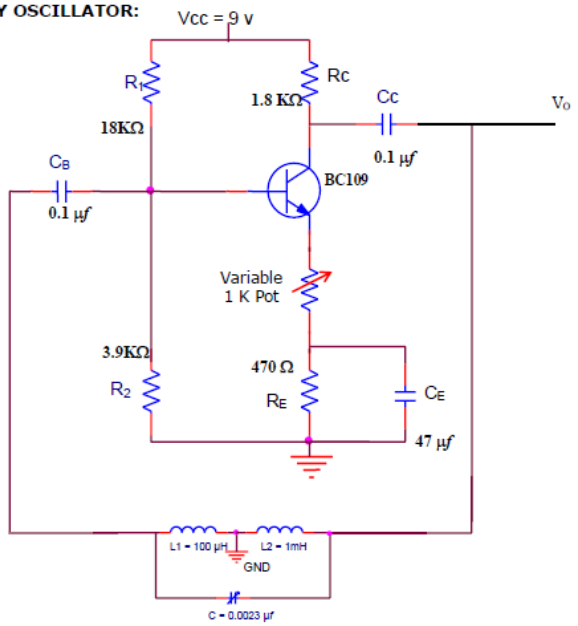
$fo = 1/ 2\pi \sqrt{L_{eq}C}$ ------where $L_{eq} = L1 + L2.$

The resonant frequency fo for Colpitts oscillator is

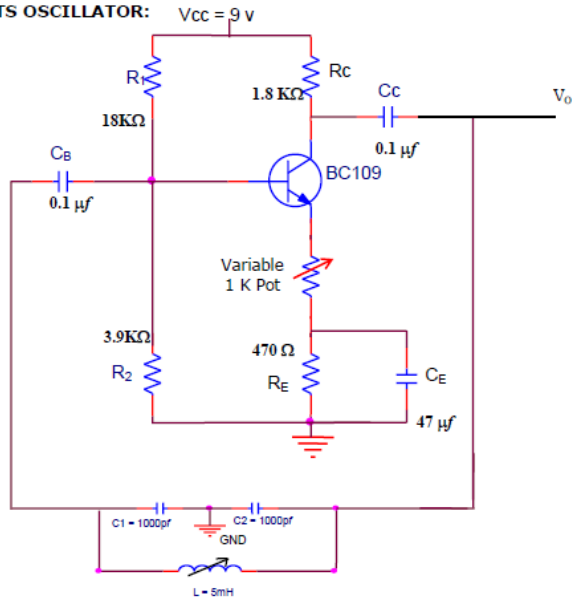
$fo = 1/ 2\pi\sqrt{LC_{eq}}$ ------where $C_{eq} = C1C2/(C1 + C2)$

CIRCUIT DIAGRAM:

HARTLEY OSCILLATOR:



COLPITTS OSCILLATOR:



DESIGN:

Given VCC = 9V, IC = 2mA, β = 50

R_E: W.K.T. $V_{RE} = V_{CC}/10 = 9/10 = 0.9V$ ------for biasing

$I_E \approx I_C = 2$ mA

From the fig. We see that,

$I_E R_E = V_{RE}$

$R_E = 0.9 / (2 \times 10^{-3}) = 450\Omega$

Therefore **$R_E \approx 470\Omega$**

R_C: $V_{CE} = V_{CC}/2 = 4.5V$ ----- for Q point to be in active region.

Applying KVL to output loop

$V_{CC} - I_C R_C - V_{CE} - V_{RE} = 0$

$9 - 2 \times 10^{-3} R_C - 4.5 - 0.9 = 0$

Therefore **$R_C = 1.8k\Omega$**

R_1 & R_2: From biasing circuit

$V_B = V_{BE} + V_{RE}$

$= 0.7 + 0.9$

$V_B = 1.6V$

Assume 10 I_B flows through R_1 and 9 I_B flows through R_2.

W.K.T. $I_C = \beta I_B$

$2 \times 10^{-3} = 50\ I_B$

Therefore $I_B = 40\ \mu A$

From the fig. we see that,

$R_1 = V_{CC} - V_B / 10\ I_B = 9 - 1.6 / (10 \times 40 \times 10^{-6}) = 18.5k\Omega$

Therefore **$R1 \approx 18k\Omega$**

$R_2 = V_B / 9I_B = 1.6 / (9 \times 40 \times 10^{-6}) = 4.44k\Omega$

Therefore **$R_2 \approx 3.9k\Omega$**

C_E, C_C, C_B: Let $C_B = C_C = 0.1\mu F$

$X_{CE} = RE/10$

Therefore $f = 10 / (2\pi C_E R_E)$

Let f = 100Hz and W.K.T $R_E = 470\Omega$

Therefore $C_E = 10 / 2\pi f.R_E = 34\mu F$

Therefore **$C_E \approx 47\mu F$.**

HARTLEY OSCILLATOR:

Attenuation $\beta = Vf/Vo = IX_{L1}/IX_{L2} = X_{L1} / X_{L2} = 2\pi foL1/2\pi foL2 = L1/L2$

For sustained oscillations $A\nu\beta = 1$ -------- $Av = 1/\beta = L2/L1$

For oscillations to start $A\nu\beta > 1$ ----------$Av > L2/L1$

COLPITTS OSCILLATOR:

Attenuation $\beta = Vf / Vo = IX_{C1}/IX_{C2} = X_{C1}/ X_{C2} = (1/ 2\pi foC1)/(1/2\pi foC2) = C1/C2$

For sustained oscillations $A\nu\beta = 1$ ---------- $Av = C1/C2$

For oscillations to start $A\nu\beta > 1$----------$Av > C1/C2$

DESIGN OF TANK CIRCUIT

Assume = fo = 100 KHz

HARTLEY OSCILLATOR

$f_o = 1/ (2\pi \sqrt{L_{eq}C})$ ------where $L_{eq} = L1 + L2$.

Assume L1 = 100 μH, L2 =1mH

$\therefore L_{EQ} =$

$\therefore f_O = 1/ (2\pi \sqrt{2*10^{-3}\ C})$

$\therefore$ C = 0.0023 μ*f* (Decade capacitance box)

COLPITTS OSCILLATOR

$f_O = 1/ (2\pi\sqrt{LC_{eq}})$ ------where $C_{eq} = (C1C2)/(C1 + C2)$

Assume C1 = C2 = 1000 pF

$\therefore$ Ceq =

$\therefore f_O = 1/ 2\pi\sqrt{L} * .05*10 - 6$

$\therefore$ L = 5 mH (Use decade inductance box)

PROCEDURE:

1. Rig up the circuit as shown in the circuit diagram.
2. Before connecting the feedback network, check the circuit for biasing conditions i.e. check VCE, and VRE.
3. After connecting the feedback network. Check the output.
4. Check for the sinusoidal waveform at output. Note down the frequency of the output waveform and check for any deviation from the designed value of the frequency.
5. To get a sinusoidal waveform adjust 1KΩ potentiometer.
6. DCB/DIB can be varied to vary the frequency of the output waveform.

TABULAR COLUMN

HARTLEY OSCILLATOR		
SL NO	C	fo

COLPITTS OSCILLATOR		
SL NO	L	fo

Waveforms

Result:

VIVA QUESTIONS:

1. What is an Oscillator?
2. What is the output of an oscillator if transistor is ideal?
3. What is Barkhausen criterion ?
4. How an oscillator generates oscillations without any input?
5. What are the output signal frequencies of different oscillators?
6. Which oscillators are AF and RF oscillators?
7. Why can't we use LC oscillator for low frequency oscillations?