JSS MAHAVIDYAPEETHA
JSS SCIENCE AND TECHNOLOGY UNIVERSITY
SRI JAYACHAMARAJENDRA COLLEGE OF ENGINEERING
- Constituent College of JSS Science and Technology University
- Approved by A.I.C.T.E
- Governed by the Grant-in-Aid Rules of Government of Karnataka
- Identified as lead institution for World Bank Assistance under TEQIP Scheme

JSS MAHAVIDYAPEETHA

JSS SCIENCE & TECHNOLOGY UNIVERSITY, MYSURU

CMOS VLSI CIRCUITS - EC630L

LAB MANUAL

for 6th Semester B.E Degree

Lab Location: AB208

Lab Incharge

Halesh M R, Asst. Professor.

Dr. Rudraswamy S B, Asst. Professor.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

2021-2022

Vision of the Institute

1. **Advancing JSS S&T University as a leader in education, research and technology on the international arena.**
2. **To provide the students a universal platform to launch their careers, vesting the industry and research community with skilled and professional workforce.**
3. **Accomplishing JSS S&T University as an epicentre for innovation, centre of excellence for research with state of the art lab facilities.**
4. **Fostering an erudite, professional forum for researchers and industrialist to coexist and to work cohesively for the growth and development of science and technology for betterment of society.**

Mission of the Institute

1. **Education, research and social outreach are the core doctrines of JSS S&T University that are responsible for accomplishment of in-depth knowledge base, professional skill and innovative technologies required to improve the socio economic conditions of the country.**
2. **Our mission is to develop JSS S&T University as a global destination for cohesive learning of engineering, science and management which are strongly supported with interdisciplinary research and academia.**
3. **JSS S&T University is committed to provide world class amenities, infrastructural and technical support to the students, staff, researchers and industrial partners to promote and protect innovations and technologies through patents and to enrich entrepreneurial endeavors.**
4. **JSS S&T University core mission is to create knowledge led economy through appropriate technologies, and to resolve societal problems by educational empowerment and ethics for better living.**

Vision statement of the department

Be a leader in providing globally acceptable education in electronics and communication engineering with emphasis on fundamentals-to-applications, creative-thinking, research and career-building.

Mission statement of the department

1. **To provide best infrastructure and up-to-date curriculum with a conducive learning environment.**
2. **To enable students to keep pace with emerging trends in Electronics and CommunicationEngineering.**
3. **To establish strong industry participation and encourage student entrepreneurship.**
4. **To promote socially relevant eco-friendly technologies and inculcate inclusive innovation activities.**

Program Educational Objectives (PEOs) of the Department

1. **To enable the graduates to have strong Engineering fundamentals in Electronics & Communication, with adequate orientation to mathematics and basic sciences.**
2. **To empower graduates to formulate, analyze, design and provide innovative solutions in Electronics and Communication, for real life problems.**
3. **To ensure that graduates have adequate exposure to research and emerging technologies through industry interaction and to inculcate professional and ethical values.**
4. **To nurture required skill sets to enable graduates to pursue successful professional career in industry, higher education, competitive exams and entrepreneurship.**

CMOS VLSI Circuits Lab – EC330L

List of Experiments:

PART – A (Digital Experiments)

1. Draw the CMOS schematic and Layout of the inverter circuit, simulate both schematic and layout to determine propagation delay, rise time fall time and Q-point and comment on the results.
2. Draw the CMOS schematic of the 2 input NAND and NOR gate, also draw the layout of the same, and simulate for transient result.
3. Draw the CMOS schematic of the Half Adder circuit and verify it with truth table, and also draw the layout of the same, and simulate for transient result.
4. Draw the CMOS circuit of the 2:1 Multiplexer circuit and verify it with truth table, and also draw the layout of the same, and simulate for transient result.

PART – B (Analog Experiments)

1. Design the Common source amplifier schematic for a gain of 30dB and also draw the layout of the same, simulate the layout for ac analysis and comment on results.
2. Design the Common Drain amplifier schematic and also draw the layout of the same, simulate the layout for ac analysis and comment on results.
3. Design the Common Gate amplifier schematic (Current Gain of 30dB) and also draw the layout of the same, simulate the layout for ac analysis and comment on results.
4. Design the Differential amplifier schematic for a gain of 50dB.

SCHEMATIC SIMULATION

PROCEDURE FOR CREATING THE SCHEMATIC SIMULATION

I. Commands to get into Cadence

1. Right Click and open the terminal window
2. Type the following commands as follows and press enter.

   i) csh
   ii) source /home/install/cshrc
   iii) virtuoso &

II. Procedure for Schematic simulation using Cadence

1. Now two windows must open i)virtuoso/command interpreter window ii)"Whats New…"
2. Close the 2nd window

3. **Use 1st window i.e virtuoso window(CIW) for further processing**.

   i) Create a New Library
   ii) Create Schematic Cell view.
   iii) Create the Symbol for schematic Cell view.
   iv) Create the test Cell view.
   v) Analog simulation by spectre

i) **Procedure for Creating New Library.**

   a. File –New – Library
   b. Name : Give name for ur library Ex: VLSILAB
   c. Enable **Attach to an existing technology library,** Click **OK**
   d. Attach the library to the technology library **gpdk180**.Click OK

ii) **Create Schematic Cell view.**

   a. Go to 1st window i.e virtuoso(CIW)
   b. File-New-Cell view

c. Setup the new file form
Library: Select the one you a created.
Cell : Give the experiment name Ex: Inverter
View: Schematic
Type: Schematic press **OK**

d. Add the required components from the libraries and make the connections.
1. Go to instance fixed menu or use shortcut key "I" from keypad to go instances
2. Click on **browse.** This opens the library browser
3. Now select the appropriate library for components like
   Gpdk180 ---------- nmos, pmos
   Analog library ---------- Vdd, Gnd, Vcc, Vpulse, Vsin
4. Make the connections by using fixed **narrow wire key**
5. Click **Check and Save** button

iii) **Creating the Symbol for schematic Cell view**

a. In the schematic window, execute
Crate – Cell view – From Cell view
The cell view from cell view window appears
Check Lib Name, Cell Name, From View name **must be schematic**
Press ok

b. Now Symbol generation form appears. Click **Ok** If No changes required

c. A new window with with default symbol is created.

d. Edit the symbol if you want to give actual symbol shape else continue.
i. Execute Create-Cell view-from cell view
ii. Library Name and Cell Name must be same which you have used for schematic. Press **OK**
iii. Check for the position of pin side.Prss **OK**
iv. Edit for the shape by Create-Shape-Choose required options to edit.

iv) **Creating the new test cell view**

a. Go to CIW window, Execute File-New-Cell view

b. Setup the new file form

Library: Select the one you a created.
Cell: **Cell name must be different from the name used in schematic cell view. Ex: Inverter_test**
View: Schematic
Type: Schematic press **OK**

c. Follow the **step 3(ii) d to** make the required connections

v) **Analog simulation by SPECTRE.**

a. In test cell view window
Launch – ADE L(Analog Design Environment)

b. Execute **Setup—Simulation/directory/Host A new window opens**

c. **Set the** simulation window **to spectre** and click **ok**

d. Execute **Setup-Model Library. Anew window opens, Check of gpdk.scs** as lib **and** section type as **stat** then press **OK.**

e. Execute **Analysis – Choose. A window opens.**

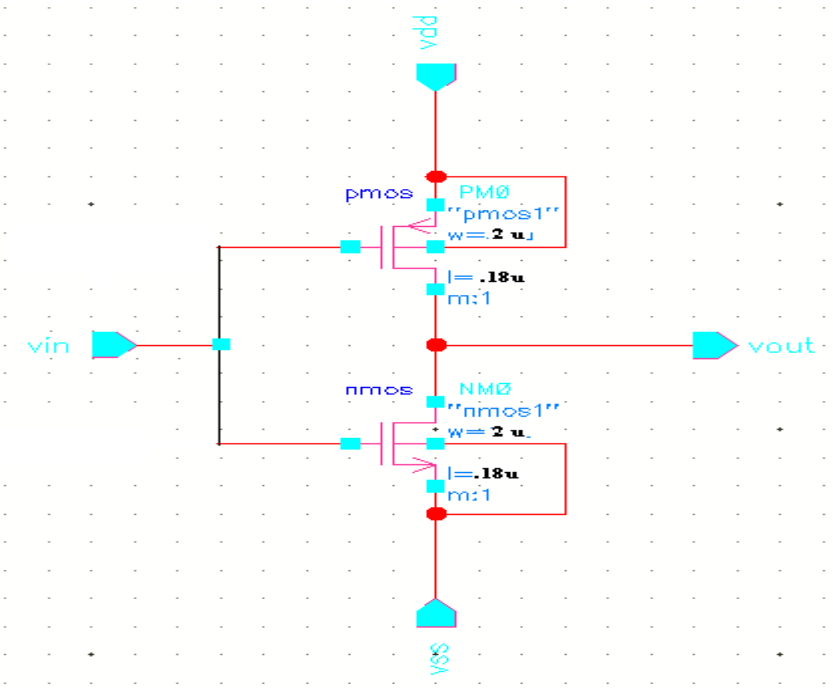
f. Select the type and set the specifications and press **OK**

g. Execute **Output s—to be plotted – Select on Schematic**

h. Then Select the **INPUT WIRE(Vin)** and **OUTPUT WIRE(Vout)** from your test Schematic using mouse

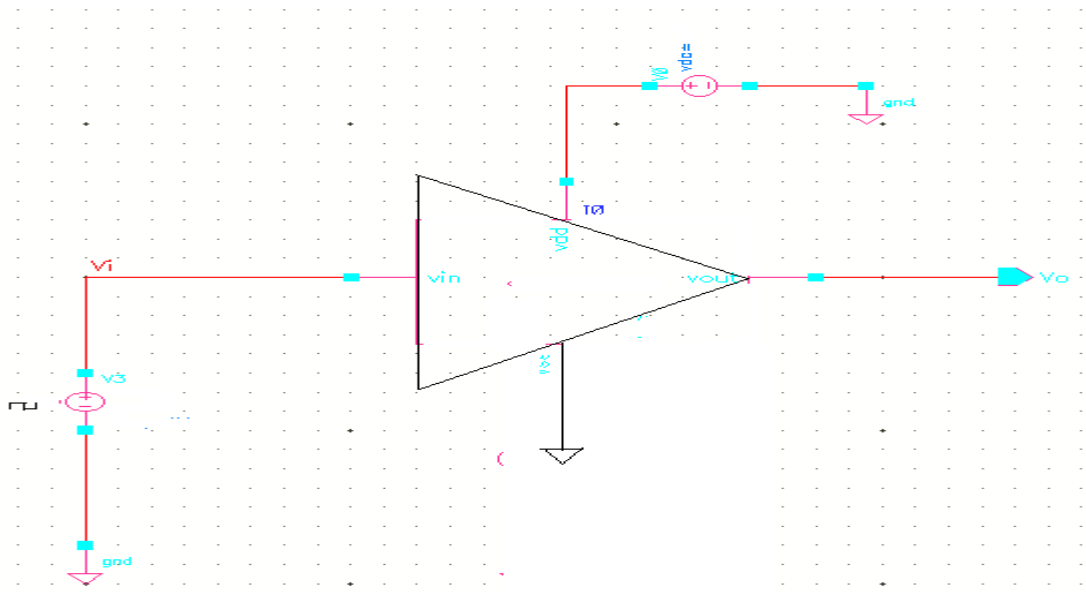
i. Execute **Simulation -- Net list and Run**

Experiment 1(a): Inverter Schematic Cell View



Specifications:

nmos	→ NM0 → W=2u L=.180U & NM1→ W=2U L=.180U
Input Pins	→ Vdd,Vss,Vin
Output pin	→ Vout



Specifications: **Vpulse →** V1 = 0 **Vdd** = 1.8
V2 = 1
td = 0,tr=tf=1 n, ton= 10n ,T=20n

Simulation Settings

Setup for transient analysis:

1. Stop time =

Setup for D.C analysis

1. Component to be selected in schematic is_____for d.c analysis
2. Start = -5 Stop = 5 resp.

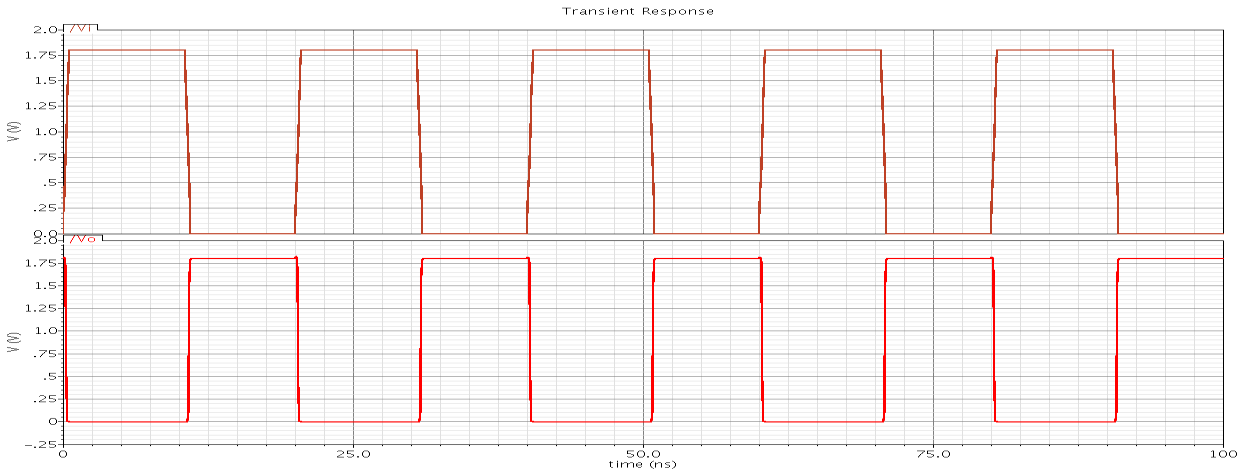
Setup for A.C analysis

1. Turn on Frequency button
2. In sweep range section – Start ____ stop _____
3. Select point per decade = _____

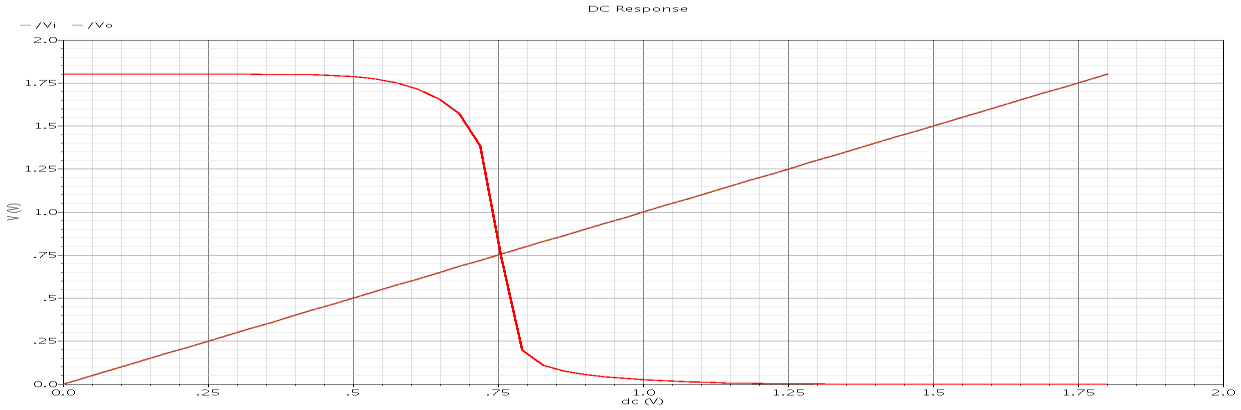
Check enables and apply

Expected Waveform:

Transient analysis

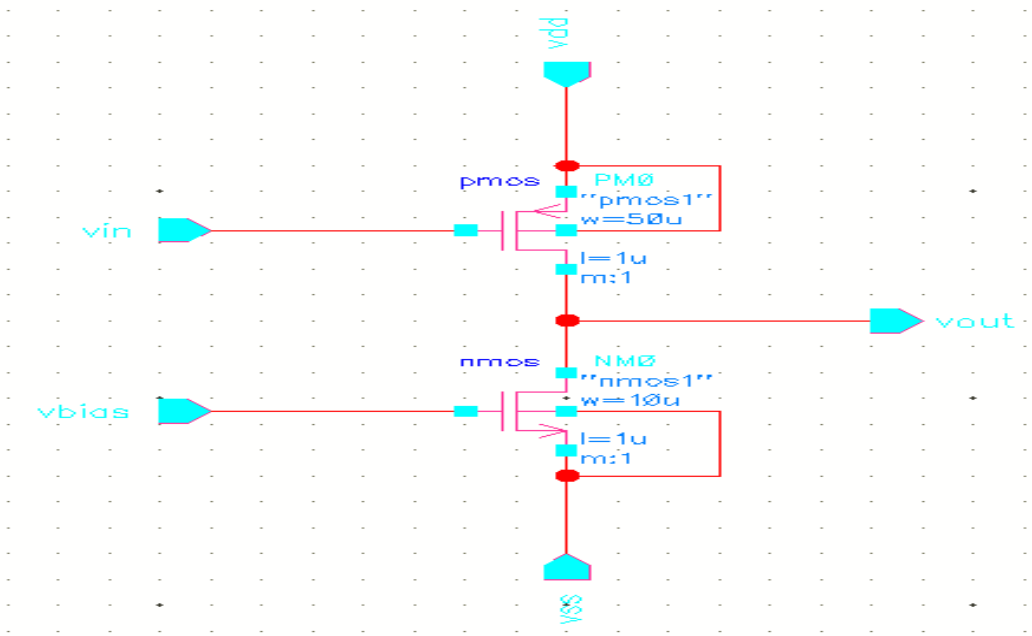


DC Analysis



Experiment 2(a): Common source Amplifier schematic Cell view

The common-source (CS) amplifier may be viewed as a transconductance amplifier or as a voltage amplifier. As a transconductance amplifier, the input voltage is seen as modulating the current going to the load. As a voltage amplifier, input voltage modulates the amount of current flowing through the FET, changing the voltage across the output resistance according to Ohm's law. The easiest way to tell if a FET is common source is to examine where the signal enters, and leaves. The remaining terminal is what is known as "common". In this example, the signal enters the gate, and exits the drain. The only terminal remaining is the source. This is a common-source FET circuit.



Specifications:

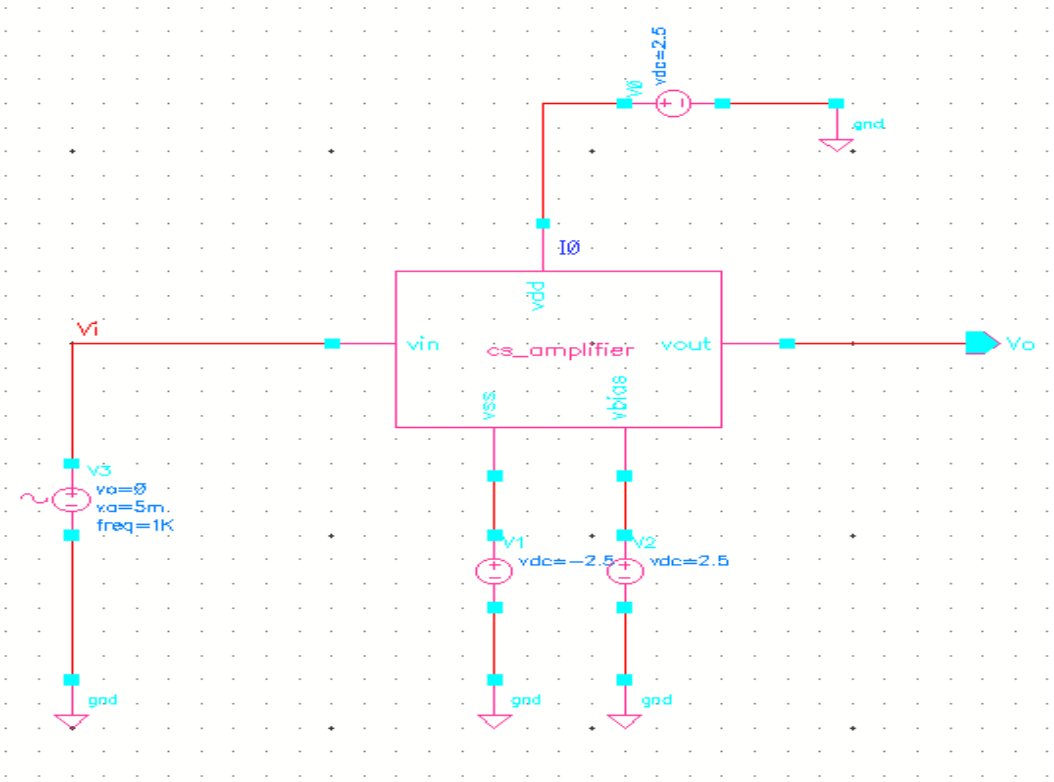
nmos	→ PM0 → W=50u L=1U
Pmos	→ NM0→ W=10U L01U
Input Pins	→ Vdd,Vss,Vin,Vbias
Output pin	→ Vout

Common source Amplifier schematic test Cellview

Specifications: **Vsin →**

a.c magnitude	= 1
d.c voltage	= 0
offset voltage	= 0
amplitude	=5m
frequency	=1K

Vdd	= 2.5
Vss	= -2.5
Vbias	= 2.5



Simulation Settings

Setup for transient analysis:

2. Stop time = 5m

Setup for D.C analysis

3. Component to be selected in schematic is Vsin for d.c analysis
4. Start = -5 Stop = 5 resp.

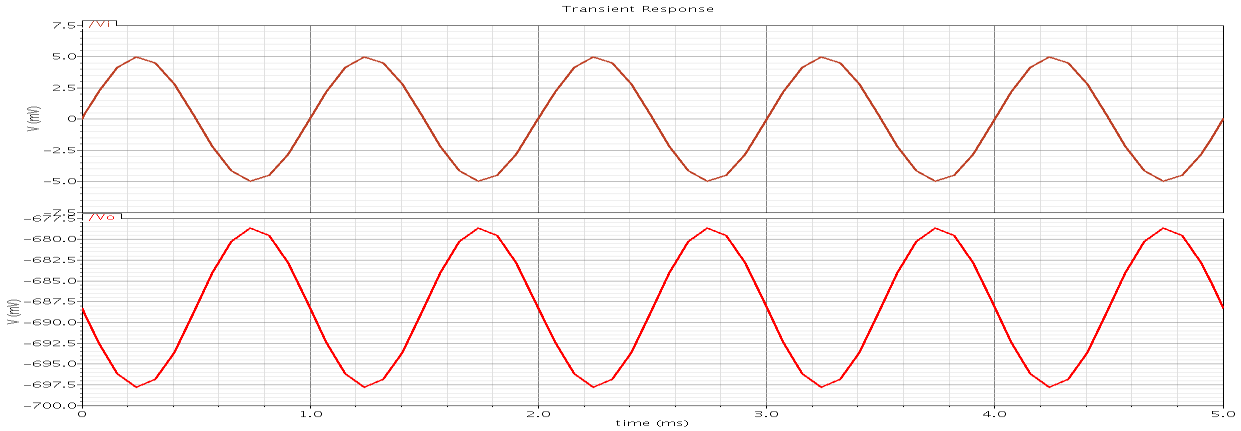
Setup for A.C analysis

4. Turn on Frequency button
5. In sweep range section – Start 7 stop – 150 to 100M
6. Select point per decade = 20

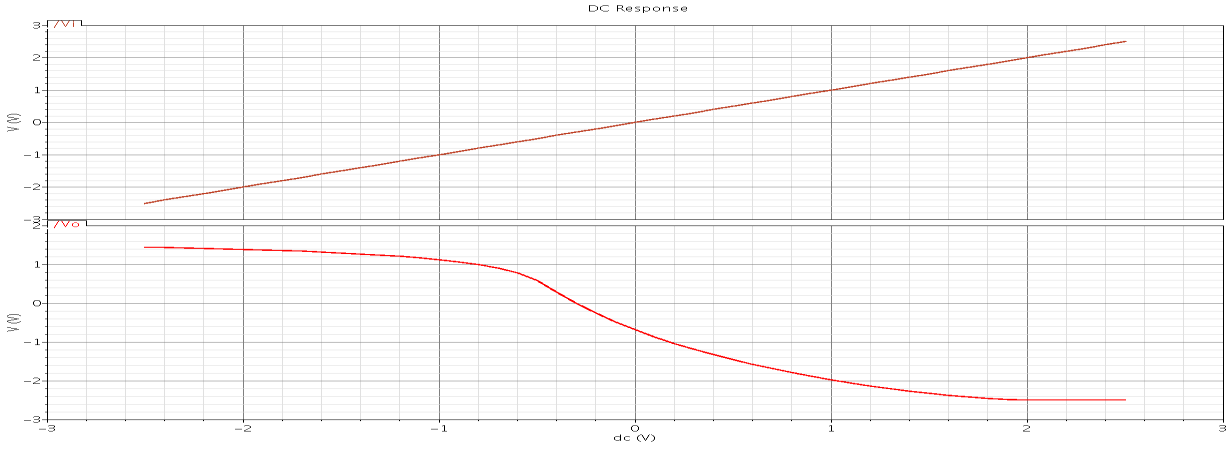
Check enables and apply

Expected Waveform:

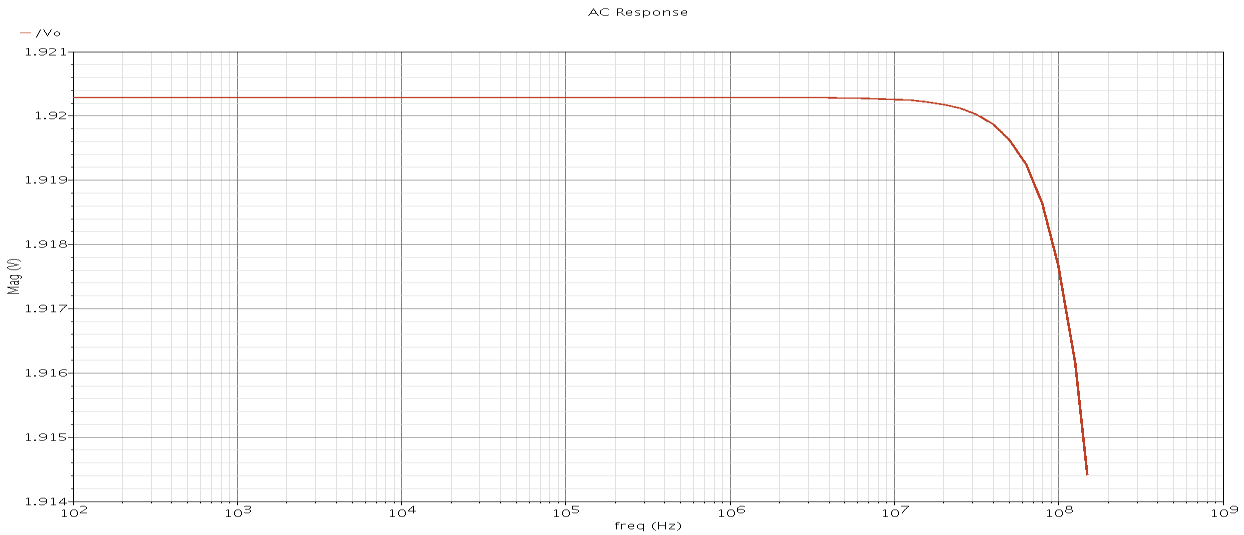
Transient analysis



DC Analysis

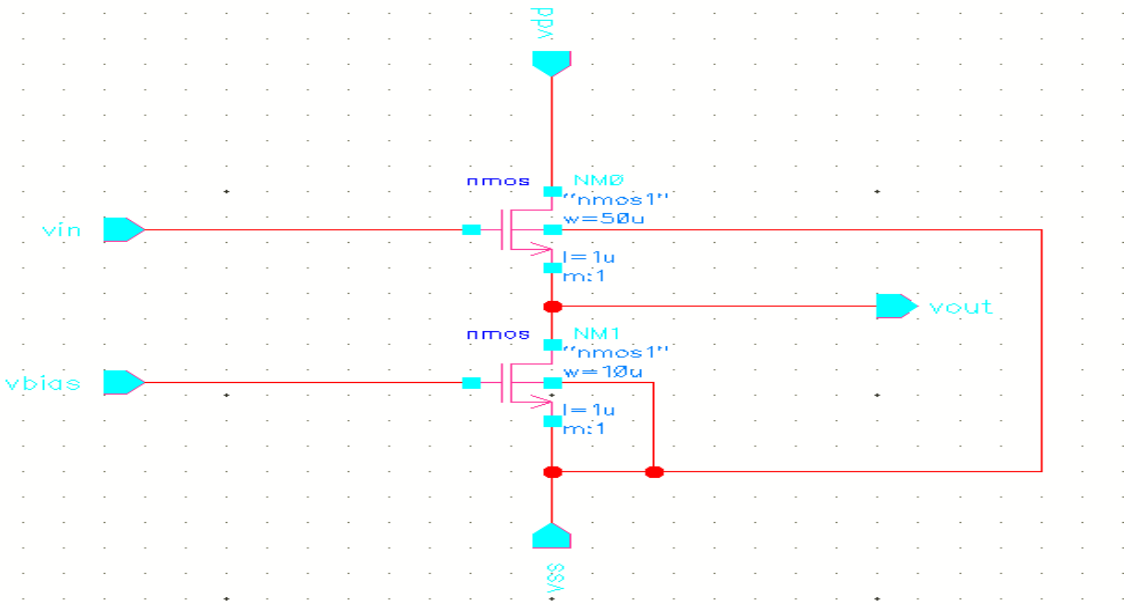


AC Analysis- Frequency



Experiment 3(a): Common drain amplifier schematic Cell view

A common-drain amplifier, also known as a source follower, is one of three basic single-stage field effect transistor (FET) amplifier topologies, typically used as a voltage buffer. In this circuit the gate terminal of the transistor serves as the input, the source is the output, and the drain is common to both (input and output), hence its name. The analogous bipolar junction transistor circuit is the common-collector amplifier. In addition, this circuit is used to transform impedances. For example, the Thévenin resistance of a combination of a voltage follower driven by a voltage source with high Thévenin resistance is reduced to only the output resistance of the voltage follower, a small resistance. That resistance reduction makes the combination a more ideal voltage source. Conversely, a voltage follower inserted between a small load resistance and a driving stage presents an infinite load to the driving stage, an advantage in coupling a voltage signal to a small load.

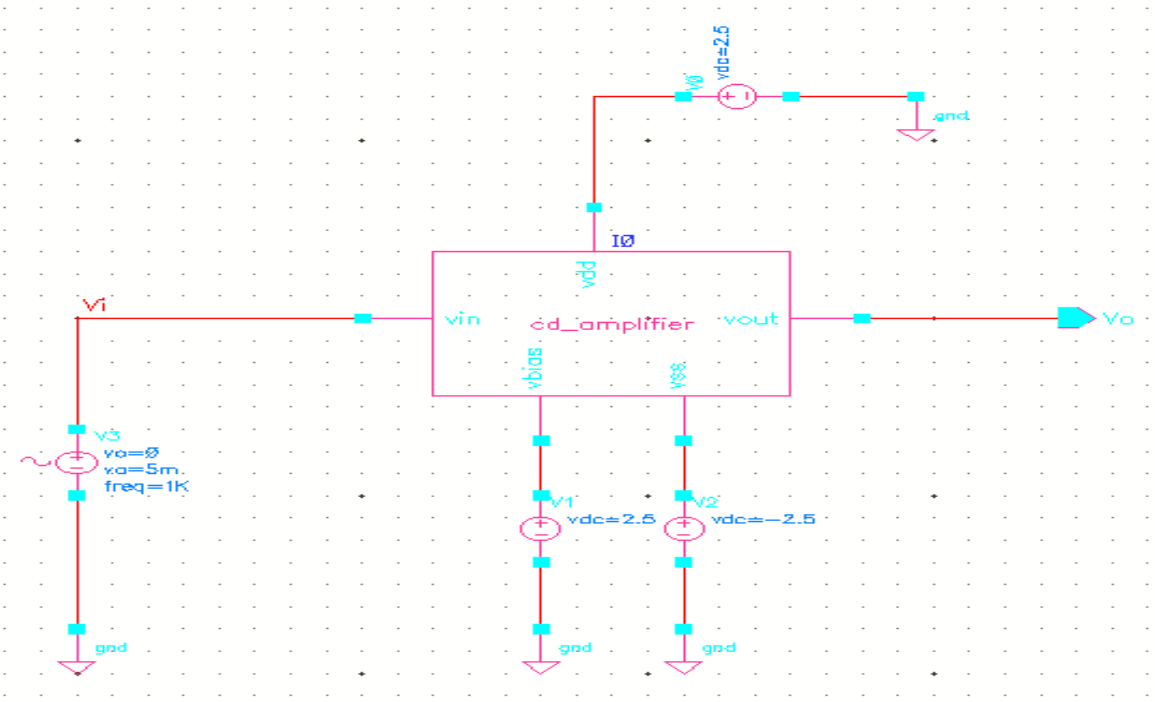


Specifications: **nmos** → NM0 → W=50u L=1U & NM1→ W=10U L=1U
Input Pins → Vdd,Vss,Vin,Vbias
Output pin → Vout

Common drain amplifier test cellview

Specifications: **Vsin →**

a.c magnitude	= 1	**Vdd**	= 2.5
d.c voltage	= 0	**Vss**	= -2.5
offset voltage	= 0	**Vbias**	= 2.5
amplitude	=5m		
frequency	=1K		



Simulation Settings

Setup for transient analysis:

1. Stop time = 5m

Setup for D.C analysis

1. Component to be selected in schematic is Vsin for d.c analysis
2. Start = -5 Stop = 5 resp.

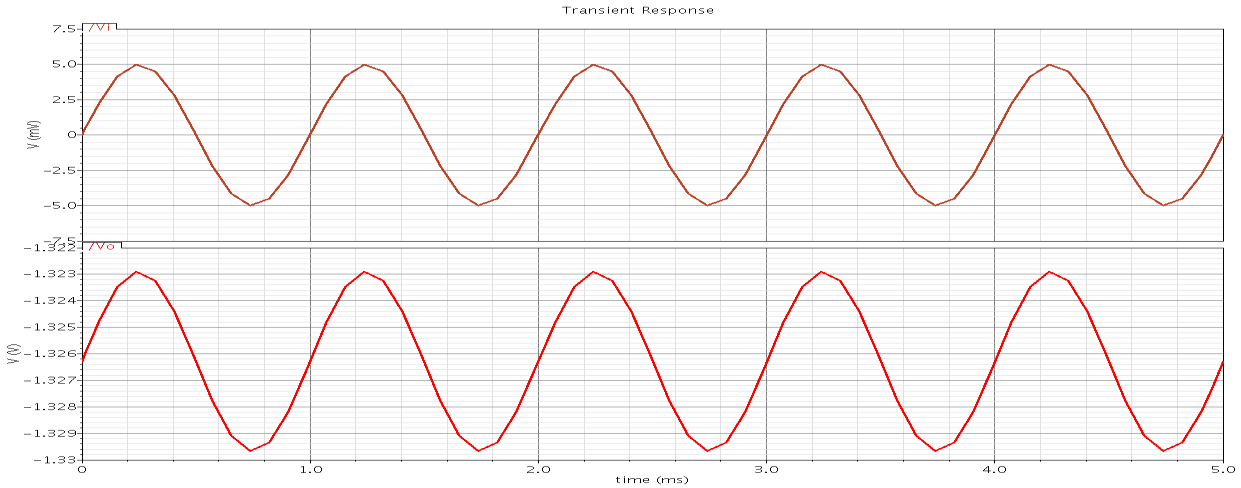
Setup for A.C analysis

1. Turn on Frequency button
2. In sweep range section – Start 7 stop – 150 to 100M
3. Select point per decade = 20

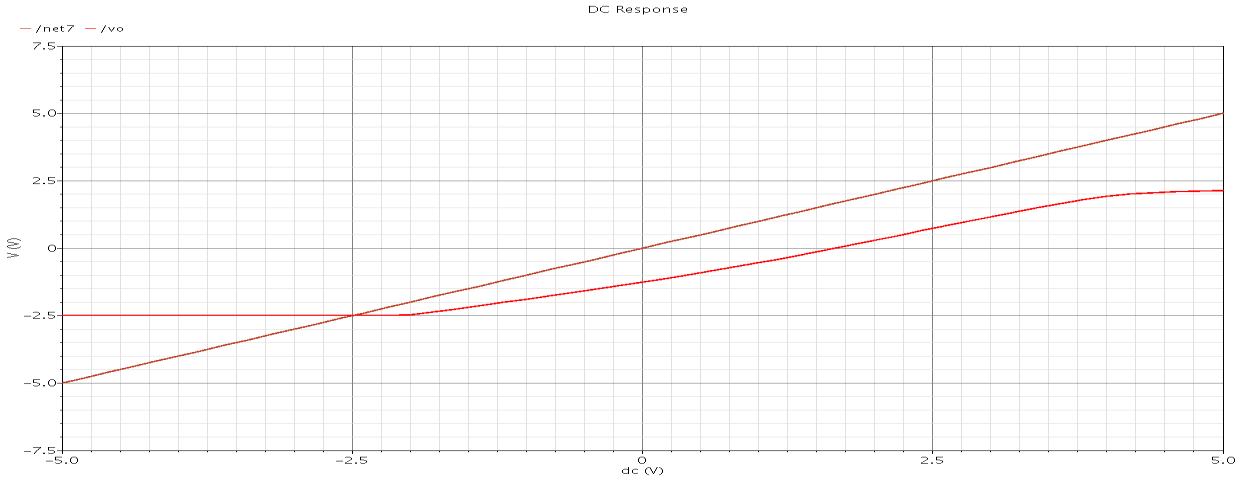
Check enables and apply

Expected Waveform:

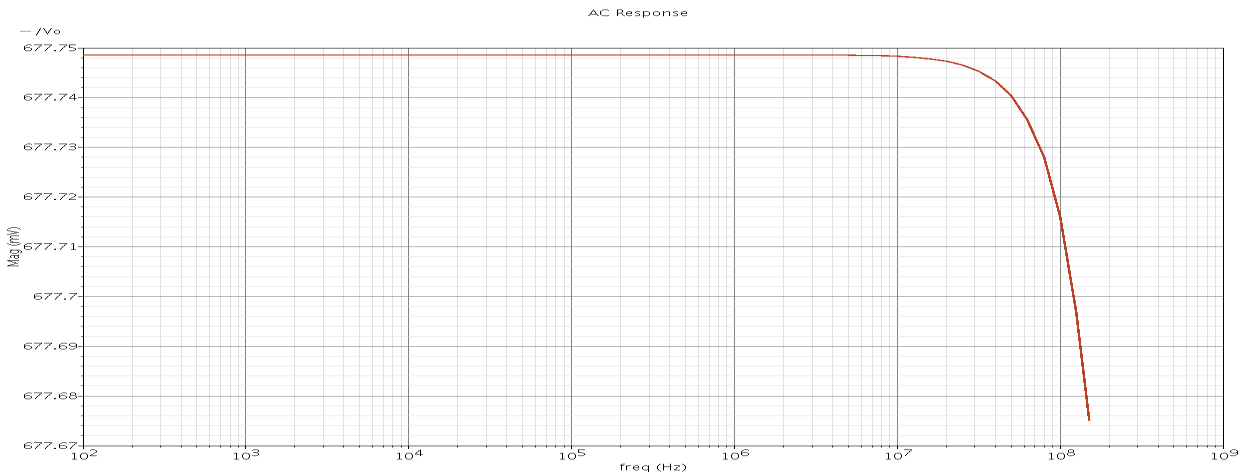
Transient analysis



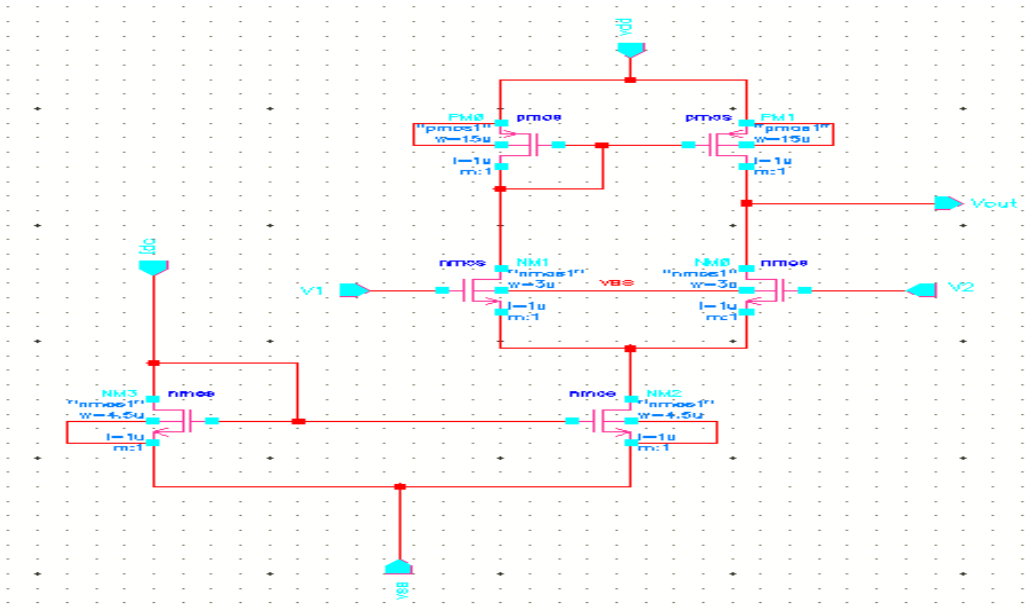
DC Analysis



AC Analysis- Frequency



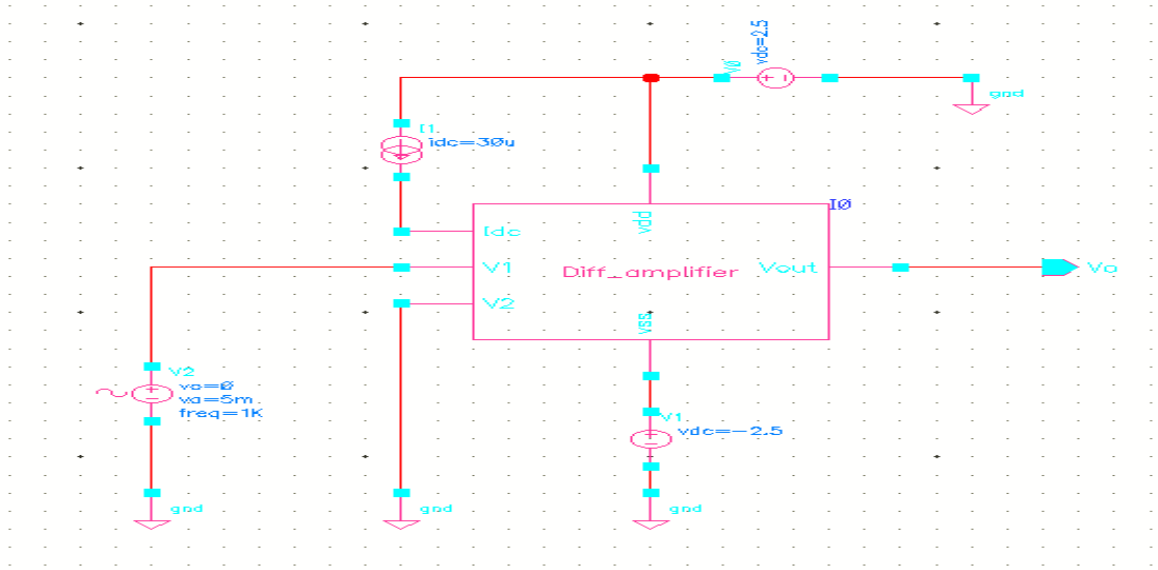
Experiment 4(a): Differential Amplifier schematic Cell view



Specifications:

nmos	→	NM0&NM1 → W=3u L=1U , NM2,NM3 → 4.5U L=1U
Pmos	→	PM0 & PM1→ W=15U L=1U
Input Pins	→	V1,V2,Idc
Output pin	→	Vout
Bidirectional pins	→	**Vdd,Vss**

Differential Amplifier schematic test Cellview



Specifications: **Vsin →** a.c magnitude = 1 **Vdd** = 2.5
amplitude =5m **Vss** = -2.5
frequency =1K **Idc** = d.c.current=30u

Simulation Settings

Setup for transient analysis:

3. Stop time = 5m

Setup for D.C analysis

5. Component to be selected in schematic is_____for d.c analysis
6. Start = -5 Stop = 5 resp.

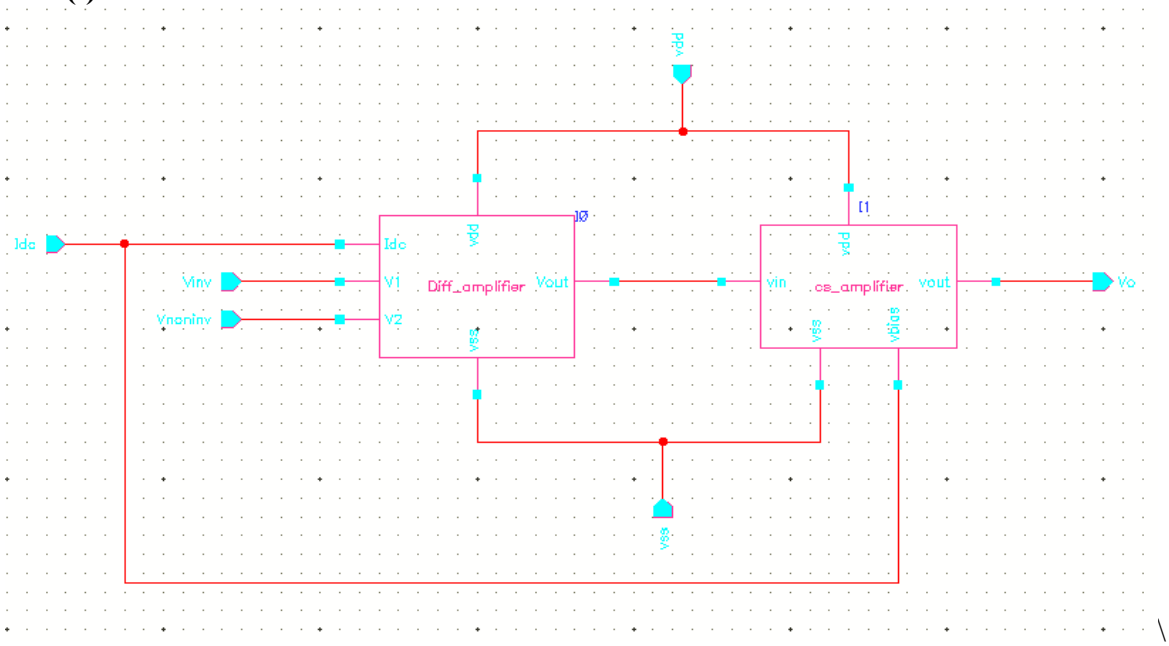
Setup for A.C analysis

7. Turn on Frequency button
8. In sweep range section – Start ____ stop _____
9. Select point per decade = _____

Check enables and apply

Expected Waveform:

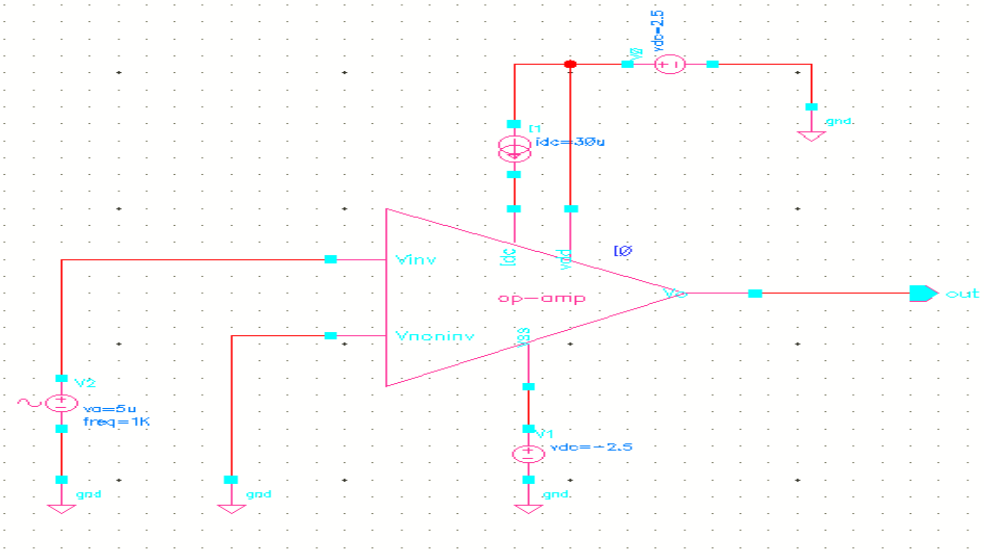
Experiment 5(a) : OPAMP schematic Cell view



Specifications:

Diff_Amplifier	→ From your library
Cs_amplifier	→ From your library
Input Pins	→ Vinv,Vnoninv,Id.c,Vdd,Vss
Output pin	→ Vout

OPAMP schematic test Cell view



Specifications: **Vsin →** a.c magnitude = 1
d.c voltage = 0
offset voltage = 0
amplitude =0.5m
frequency =1K

Vdd = 5
Vss = -2.5
Idc = d.c current=30 u

Simulation Settings

Setup for transient analysis:

4. Stop time =

Setup for D.C analysis

7. Component to be selected in schematic is_____for d.c analysis
8. Start = -5 Stop = 5 resp.

Setup for A.C analysis

10. Turn on Frequency button
11. In sweep range section – Start ____ stop _____
12. Select point per decade = _____

Check enables and apply

Expected Waveform: