JSS MAHAVIDYAPEETHA
JSS SCIENCE AND TECHNOLOGY UNIVERSITY
SRI JAYACHAMARAJENDRA COLLEGE OF ENGINEERING
• Constituent College of JSS Science and Technology University
• Approved by A.I.C.T.E
• Governed by the Grant-in-Aid Rules of Government of Karnataka
• Identified as lead institution for World Bank Assistance under TEQIP Scheme

Department of Electronics and Communication Engineering

Semester wise Lab manual Details

SI.No	Semester	Lab Manual
1	III SEM	1. Analog Electronics Circuits Lab 2. HSIS Lab 3. Digital System Design Lab
2	IV SEM	1. Microcontrollers Lab 2. Communication Lab -I 3. Linear Integrated Circuit Lab
3	V SEM	1. Communication Lab-II 2. Digital Signal Processing Lab
4	VI SEM	1. Computer Networks Lab 2. VLSI Lab 3. Design and Implementation Lab
5	VII SEM	Power Electronics Lab

Signature of HoD

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